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Our cover photo shows two of this month's featured products doing one of their principal jobs, testing telephone equipment. A frequency division multiplex (FDM) telephone system like the one on the cover carries many telephone channels, each spanning a frequency range of 0 to 4000 Hz, stacked one on top of another in frequency. Thus the composite signal transmitted from point to point over microwave radio links is a broadband signal with its energy spread out over a wide range of frequencies. In testing a system like this, it's often necessary to measure how much energy is in one particular channel or part of a channel. That's the job of a selective level meter like Model 3586A/B/C (page 3). It *selects* the narrow band of frequencies the user wants to measure, and then it *meters* the signal *level* (the amount of energy) in that narrow band. Sometimes it's useful to send a precise tone over a channel and measure what happens to it with a selective level meter. Generating that tone with a precise frequency and magnitude is the job of Model 3336A/B/C Synthesizer/Level Generator (page 9). The A and B versions of the 3586A/B/C and 3336A/B/C are designed especially for telephone testing in Europe and North America. And since there are many other uses for such instruments besides telephone testing, there's a C version of each one for general-purpose design, manufacturing and maintenance applications. (We're grateful to Southern Pacific Communications Company for allowing us to use their FDM equipment as a backdrop for our cover photo.)

Rounding out this month's issue are two logic state analyzer articles. Logic state analyzers are used for checking information flow in digital systems such as computers and microprocessors. Model 1610A has been Hewlett-Packard's most capable general-purpose logic state analyzer. Now there's a new version, Model 1610B, that offers more flexibility in how data is captured (page 14). For example, in some microprocessors, the addresses of memory locations and the data stored in those locations appear on the same bus, but at different times. Model 1610B can catch them both and display them side by side.

Model 1611A Logic State Analyzer is designed specifically for testing microprocessors. You can customize it to test a particular microprocessor by plugging in a personality module. Several personality modules are available, one for each of the more widely used microprocessors. Unlike these, the latest module, Option 001, isn't designed for any particular microprocessor, but instead turns the 1611A into a general-purpose microprocessor analyzer. This story starts on page 19.

-R. P. Dolan

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A Programmable Selective Level Meter (Wave Analyzer) with Synthesized Tuning, Autoranging, and Automatic Calibration

Covering an input frequency range of 50 Hz to 32.5 MHz, this tuned voltmeter measures characteristics of both the voice channels and the multiplexed channels of FDM communications systems. An alternate version functions as a general-purpose wave analyzer.

by Paul L. Thomas

INSTRUMENTS THAT CAN TUNE OUT all but one frequency component in a complex signal and measure the component's amplitude precisely are known as selective level meters or wave analyzers—terms that have practically become synonymous.

If there has been any difference between a wave analyzer and a selective level meter (SLM) it is that the SLM is optimized with the appropriate bandwidths and input impedance levels for telephone system measurements while the wave analyzer is designed for general-purpose use on all kinds of signals. The SLM is designed to select and measure a particular telephone channel or pilot tone in an FDM (frequency division multiplexed) communications system.

Spectrum analyzers, another kind of instrument, also separate the frequency components of a signal for analysis, but since they display all components within a selected frequency range at the same time, they are designed for wide dynamic display range and therefore have more difficulty in achieving the amplitude measurement accuracy that SLM/wave analyzers are capable of achieving.*

*A fundamental difference between wave and spectrum analyzers is in the shapes of the filter responses. Spectrum analyzers need filters with Gaussian-shaped response so the filters won't ring as the tuning sweeps a signal through the filter's passband. A wave analyzer's filters, on the other hand, can have steeper skirts since the signal usually remains in the passband long enough for transients to settle down, and the top of the response curve is flattened to allow for a slight amount of mistuning.

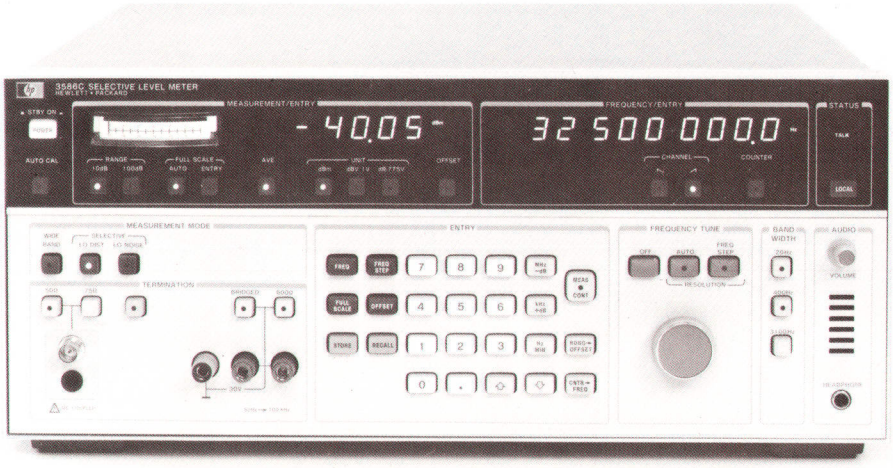

Fig. 1. *Model 3586A/B/C Selective Level Meter (3586C shown) is designed for general-purpose wave analysis and telecommunications applications including audio, sonar, radio, and frequency division multiplex (FDM) systems testing. It has a frequency range of 50 Hz to 32.5 MHz, ±0.2-dB level accuracy, and 0.1-Hz frequency resolution.*

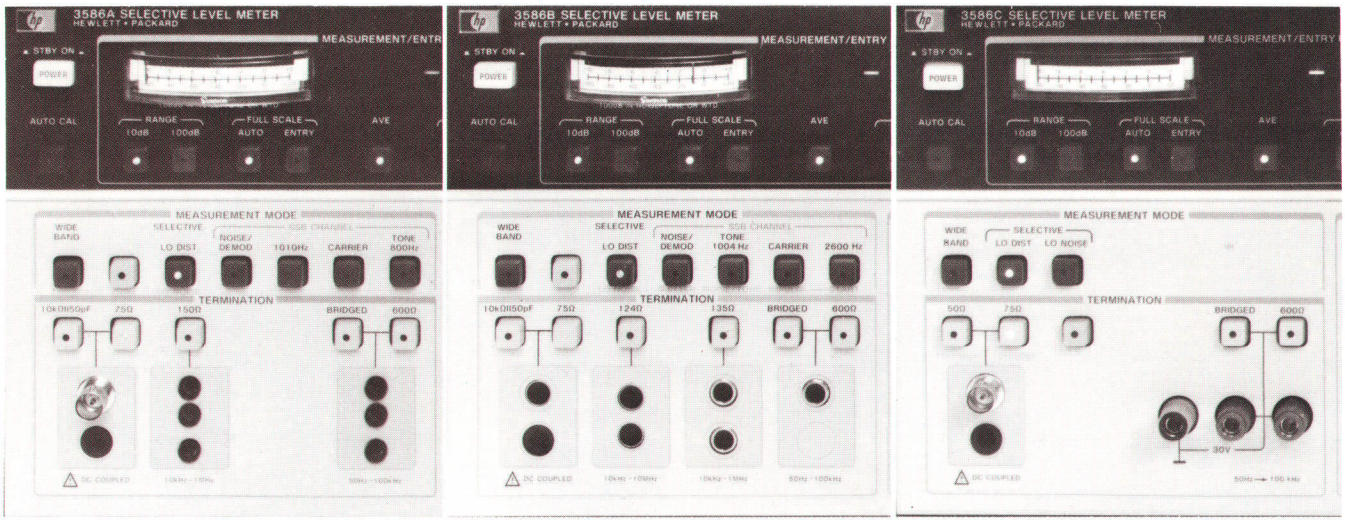

Fig. 2. *A, B, and C versions of the 3586 Selective Level Meter differ in their input configurations and internal filters. Model 3586A meets CCITT requirements; Model 3586B is for North American (Bell) applications, and Model 3586C is for general-purpose wave analysis.*

Hewlett-Packard has been designing and manufacturing wave analyzers for years, some of which (the 312C and 312D) are optimized for telephone applications. New SLMs and wave analyzers are now being designed around microprocessors to achieve greatly enhanced capabilities. The first of the new microprocessor-controlled generation of SLMs was the Model 3745A Selective Level Measuring Set,[1] introduced in 1975. This instrument greatly reduces the time needed to tune to a particular channel or pilot tone in an FDM system by having tables of the 3600 or so FDM frequencies stored in read-only memory (ROM). The operator tunes the instrument to the proper frequency simply by entering a description of the desired channel (channel number, group number, supergroup number, etc.) by way of the keyboard. The microprocessor looks up the correct frequency for the selected measurement on that channel and then, by control of the synthesized first local oscillator, tunes the analyzer accordingly. This plus autoranging greatly speeds measurements of gain, loss, noise, and other characteristics of telephone systems. It also enables the instrument to be readily incorporated into automatic systems.

A lower-cost microprocessor-controlled SLM has now been designed for use in laboratory, production test, and system maintenance applications. This one, Model 3586A/B/C (Fig. 1), is tuned manually, but as we shall see, microprocessor control simplifies its tuning and gives it other convenience features such as full remote control through the HP interface bus (HP-IB).*

An Overview

The new Model 3586A/B/C Selective Level Meter has a frequency range of 50 Hz to 32.5 MHz, covering both the telephone voice band and multiplexed channel frequencies.** The user may thus compare measurements made on the same channel at both the voice-frequency and multiplexed levels. A synthesized local oscillator makes it possible to set the frequency tuning with 0.1-Hz resolution. A built-in counter measures the frequency of an unknown signal accurately so the instrument can be tuned exactly to that frequency without the necessity to spend time "rocking" the tuning control to center the signal in the instrument's passband.

The amplitude measurement range is from +25 to −125 dBm with errors less than ±0.2 dB over the major part of the instrument's input range. Autoranging permits use of a 10-dB display range, giving an amplitude measurement resolution of 0.01 dB for examining the fine-grain frequency response of telephone channels.

The microprocessor scales the measured quantity so results are displayed in the units selected (dBm, dBpW, or dBV referred to 0.775V). A reference reading may be stored as an offset by use of the RDNG→OFFSET key so relative measurements may be made, for example, with respect to the test level point (TLP) or the fundamental frequency component of a signal. Any other reference value may also be stored as an offset using the numeric keypad.

Automatic calibration to an internal standard every three minutes and use of a true-rms detector assure accuracy in both tone and noise measurements. The instrument can also measure the total power in broadband signals applied to its input, giving a quick indication of the power level of a multiplexed signal.

To meet the requirements of a broad range of applications, several input configurations are provided. Model 3586A, intended for use in CCITT-compatible telephone systems, has a 75Ω/10kΩ single-ended input using a BNC connector, and 150Ω and 600Ω balanced inputs using Siemens 3-prong connectors (Fig. 2). These input configurations are suitable for connecting the instrument to various levels within the FDM hierarchy.

Model 3586B, for Bell-compatible systems, has a 75Ω single-ended input and 124Ω, 135Ω, and 600Ω balanced inputs with appropriate WECO connectors.

Model 3586C, intended for general-purpose wave-analyzer applications, has a single-ended 50Ω/75Ω input

*Compatible with ANSI/IEEE 488-1978.

**The instrument is usable down to 10 Hz with unspecified performance.

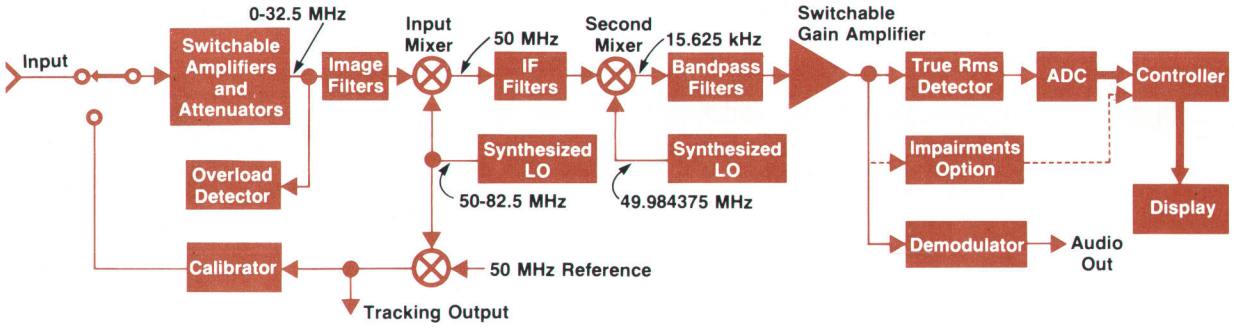

Fig. 3. *The 3586A/B/C is a dual-conversion superheterodyne receiver. Resolution bandwidth is determined by the second-IF filters.*

using a BNC connector, and a 600Ω balanced input using a dual-banana connector.

Other impedance-connector combinations are available for any of the versions. All provide probe power at the front panel for wideband, high-impedance, active probes.

Filter bandwidths of 20 Hz and 400 Hz are standard on all versions, and 3100 Hz is optional. Model 3586A (CCITT) also includes a 1740-Hz psophometric equivalent noise-weighting filter, and Model 3586B (Bell) includes a 2000-Hz C-message equivalent noise-weighting filter so measurements made with these instruments can be related to traditional noise measurements on telephone systems. The transmission impairments measurement option includes a highly selective 3100-Hz channel filter plus a true psophometric or C-message noise weighting filter for more accurate noise level measurements. With this option, the telephone-oriented versions can make transmission impairment measurements such as noise-with-tone, signal-to-noise-with-tone ratio, phase jitter, and single-level impulse noise. Because of their extended frequency range, the instruments are capable of making these measurements at the multiplex level as well as at voice frequencies.

All versions also work with the Model 3336A/B/C Synthesizer/Level Generator (see page 9). This instrument generates sine waves with accurately-controlled amplitude levels. Its tuning can be controlled by the 3586A/B/C SLM through the HP Interface Bus to function as a tracking signal source for measurements made with the 3586A/B/C. The 3586A/B/C SLM itself has a tracking output, useful for frequency-response measurements but lacking the level settability of the 3336A/B/C.

Semiautomated Tuning

To tune the 3586A/B/C, the operator enters the desired frequency through the numeric keyboard. To change the tuning, the operator can enter a new number or use the up-down step keys or the rotary tuning knob. The amount by which the step keys and tuning knob change the frequency can be selected with 0.1-Hz resolution by entering the desired step value through the numeric keypad and pressing the FREQ STEP key. One can enter the frequency being measured as the frequency step, for example, and then step from harmonic to harmonic, or enter 4 kHz and step from one channel of an FDM signal to the next.

When measurements are being made on multiplexed telephone channels, the user need only enter the carrier frequency for that channel, then indicate whether the channel signal is in the upper or lower sideband, using the ◿ (upper) or ◺ (lower) key. The instrument's tuning is automatically offset the exact 1850 Hz needed to center the tuning in the selected sideband. Other keys can be used to offset the tuning to center the tuning on the channel test tones (800/1010 Hz for CCITT, 1004/2600 Hz for Bell). In each case it is not necessary to enter a nine-digit number to change the frequency—simply pressing the appropriate key changes the tuning by the required amount, saving much time in evaluating the performance of an FDM system.

Tuning the instrument to a signal whose frequency is not known exactly is easily done by tuning the instrument approximately by any of the procedures just described and then pressing the COUNTER button. The counter will measure the largest signal within the selected bandwidth. Pressing the CNTR→FREQ button then tunes the analyzer to the displayed counter frequency.

Level Measurements

Measurements of signal level have also been made easier with microprocessor control of autoranging. As with any wave or spectrum analyzer, the 3586A/B/C has a broadband input attenuator, as indicated in the block diagram of Fig. 3, whose purpose is to reduce the signal input to a level that assures that the largest signal component does not overdrive or damage the input amplifier and mixer. The control for this attenuator on other analyzers is usually labeled INPUT SENSITIVITY, REFERENCE LEVEL, or MAXIMUM INPUT LEVEL. Then there is an IF gain control, usually called RANGE, that adjusts the IF gain to bring the selected signal component up to a suitable level for the detector. Obviously there are many combinations of the settings for these two controls that will bring the selected signal component up to a suitable detector level. For highest accuracy, however, the best combination is the one that uses the least attenuation at the input.

The 3586A/B/C has a broadband rms detector at the input that senses the input level and sends this information to the microprocessor.* The microprocessor then selects one of the eleven input attenuator steps accordingly. The microprocessor is also sent the IF signal level sensed by the IF detector, and uses this information to select one of the

*The rms value is considered a better overload indicator for an SLM than the peak or average value, since the many frequency components of a multiplexed telephone signal, each of which by itself is several dB below the composite power level, could add up vectorially to high peak values at random times. The rms value permits the input attenuator to be set to a more sensitive range. The occasional overload peaks do not affect operation of the Model 3586A/B/C significantly.

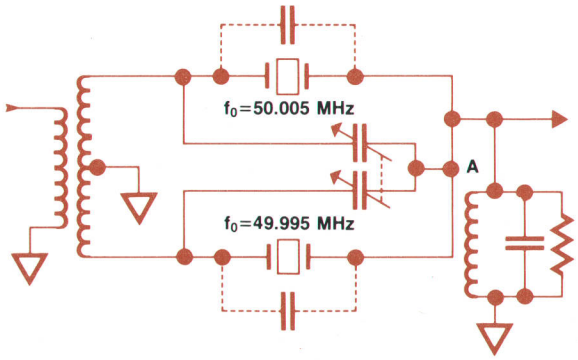

Fig. 4. *Crystals in the 1st IF filter are stagger-tuned to achieve the desired bandwidth. However, at 49.96875 MHz, the currents through the shunt capacitances of the two crystals are exactly equal and of opposite phase, cancelling at point A to give a transmission zero at 49.96875 MHz.*

eighteen gain steps to place the IF signal level within the detector's most linear 10-dB range. This assures maximum accuracy in the measurements. The user may, however, freeze either the input attenuator and/or the IF gain at any selected level for special measurement situations, such as scanning a spectrum to observe relative levels, or when using another instrument to make transmission impairment measurements on the demodulated output (the appropriate carrier may be reinserted to demodulate a channel for further analysis).

Two Conversions

As shown in the block diagram of Fig. 3, the 3586A/B/C is a dual-conversion, superheterodyne receiver. The first conversion up-converts the input signal to an intermediate frequency of 50 MHz. This up-conversion places the image frequencies in a range of 100 to 132.5 MHz where they are easily suppressed by low-pass filtering.

The final IF frequency is 15.625 kHz.* In the traditional analyzer, a down-conversion from 50 MHz to 15 kHz would be accomplished in two or three down-conversion steps so that adequate separation can be maintained between the IF and its image at each down-conversion. However, minimizing the number of down-conversions is desirable because each down-conversion inevitably introduces some noise, phase instabilities, and harmonic distortion. Although individually these can be held to very low levels, the total obtained with several down-conversions may not be insignificant, not to mention the cost of an additional local oscillator and mixer for each conversion.

In the 3586A/B/C, down-conversion from the first IF to the final IF is accomplished in only one step. This was made possible by the use of a special type of filter for the first IF. Similar to a filter used in the Model 3571A Tracking Spectrum Analyzer,[2] this filter, diagrammed in Fig. 4, passes the 50-MHz first IF signal with little insertion loss, but it has a sharp null at 49.96875 MHz where the image frequency lies. Two filters in cascade suppress the image by greater than 80 dB.

The second IF filters provide the resolution bandwidth. The 20-Hz filter (20 Hz at the 3-dB points) has a Butterworth shape and is flat within ±0.3 dB in the 6-Hz central portion of the response curve so a minor amount of frequency instability can be tolerated in the measured signal. The filter suppresses tones 80 Hz above and below the center frequency by more than 50 dB. Hence, the filter can suppress a carrier at 104.00 kHz while passing a pilot at 104.08 kHz for measurement.

The 400-Hz filter, a traditional value in selective level meters, responds faster than the 20-Hz filter so is useful when searching for a signal.

The 1740-Hz (CCITT) and 2000-Hz (Bell) filters are similar to those used for many years in the measurement of equivalent noise in a telephone channel. These filters are centered at 1350 and 1500 Hz, respectively, from the lower end of the channel, so that their passbands begin at or near 500 Hz, an important area for voice fidelity. The 3100-Hz filter—standard in the 3586C, an optional replacement for the 1740-Hz or 2000-Hz filter in the 3586A/B—is centered at 1850 Hz. This filter simulates an actual multiplexed channel filter. It has extremely steep response slopes (Fig. 5),

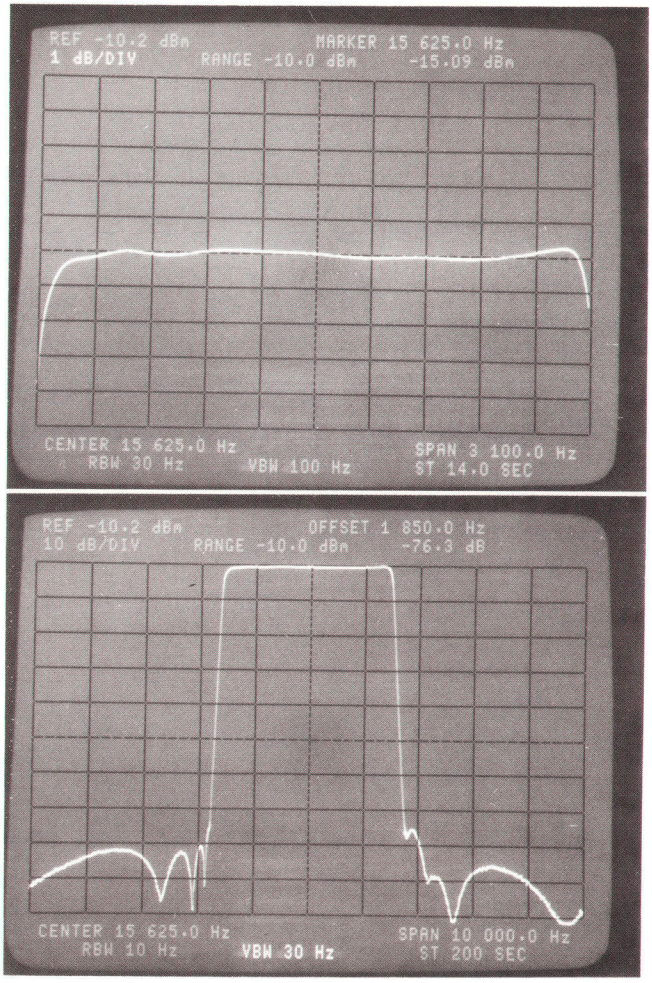

Fig. 5. *Optional 3100 Hz filter simulates a multiplexed channel filter. It provides a flat response over ±1000 Hz and has high selectivity. These photos demonstrate its flatness, carrier rejection (−76.3 dB at 1850 Hz offset, and adjacent channel rejection (>80 dB).*

*A frequency in this range was chosen because of the availability of suitable crystals for the bandpass filters. The specific value was chosen because a carrier reference signal of 15.625 kHz is obtained from a 1-MHz reference simply by use of a ÷64 digital IC.

giving the filter a shape factor of 1.2 (ratio of response curve width at −60 dB to width at −3 dB). The first cusp of all three filters lies exactly at the carrier frequency (±1350, ±1500, or ±1850 Hz from the center), thus suppressing any carrier leak. In the 3586A/B, the noise filters included with this option are weighted according to the CCITT psophometric curve or the Bell C-message curve.

Quiet, Precise Local Oscillator

A key element in any wave or spectrum analyzer is the first local oscillator. Any noise or frequency instability in this oscillator becomes impressed upon the input signal during the first frequency conversion. The 3586A/B/C uses a synthesizer as the first local oscillator, thus obtaining frequency accuracy and stability. Exceptionally low noise and low spurious are achieved by use of the fractional-N technique,[3] which provides nine-digit frequency resolution with only three phase-locked loops in the synthesizer.

A block diagram of the synthesizer is shown in Fig. 6. The 50-to-82.5-MHz first LO signal, f_o, is taken from the voltage-controlled oscillator (VCO) in the summing loop. This oscillator is locked to both the step-loop and the fine-loop frequencies, f_s and f_f respectively.

The VCO in the step loop operates within a frequency range of 54 to 86 MHz. Its output, f_s, is divided down in MECL circuits to 2 MHz by a factor N, where N is an integer between 27 and 43. The 2-MHz divided-down step loop output is compared to a 2-MHz reference in a phase comparator to derive a control signal that locks the VCO such that $f_s/N=2$ MHz. Note that this is equivalent to multiplying the 2-MHz reference by a factor N and that the phase noise multiplication factor increases by only 20 $\log_{10}$ (43/27), ≈ 4 dB across the entire range. Phase noise is only about −118 dBc/Hz anywhere in the instrument's frequency range. This is important in a highly selective SLM because phase noise in the local oscillator becomes impressed on the signal and has the effect of broadening the filter passbands. The 3586A/B/C's phase noise is low enough that even a large tone in an adjacent channel will be suppressed by more than 80 dB with the 3100-Hz filter (10 $\log_{10}$ 3100 − 118 = −83 dB).

The fine-loop frequency originates in a fractional-N loop similar to the one used in the Model 3336A Synthesizer/Level Generator (see page 9). This loop generates a frequency in the range of 20 to 40 MHz with eight-digit resolution. It is divided by 10 to obtain a signal, f_f, in a range of 2 to 4 MHz that is compared in a phase detector to the difference between f_o and f_s, the output and step-loop frequencies. The output of the phase detector thus locks the summing-loop VCO such that the output frequency, f_o, equals f_s-f_f, the difference between the step-loop and fine-loop frequencies.

To obtain nine-digit resolution without the fractional-N technique, more loops would have been required with a consequent increase in the quantity of spurious mixing products, as well as in cost.

Wideband Rms Detector

For accuracy in making measurements on the complex signals encountered in communications systems, it was considered desirable to use a detector that responds to the rms value of the measured waveform. The requirement of an 80-dB dynamic range ruled out thermocouples and a number of other rms detectors. A commercially available IC rms-to-dc converter was found that has desirable properties, such as low cost and both log and linear outputs, but a range of only 40 dB. It was therefore decided to devise a circuit that would compress an 80-dB signal range to 40 dB, and then adjust the display reading accordingly.

A simplified diagram of the circuit is shown in Fig. 7. The input goes to an operational amplifier. The output of the amplifier is applied to the rms-to-dc converter, and the resulting dc current is coupled back to the input of the operational amplifier. The output of this amplifier thus has two components: an ac component, e_o, that results from the signal input, and a dc output, V_o, that results from conversion of the signal's rms value to dc.

The dc component is applied to an integrator that drives a light-emitting diode. The diode in turn illuminates a photoresistor, R_F, in the feedback loop of the input operational amplifier, adjusting R_F to maintain the dc voltage drop through R_F constant such that V_o is always equal to V_R at the input to the integrator. R_F, and hence the gain of the operational amplifier, varies inversely with the rms signal level, making e_o proportional to the square root of e_i, the input voltage. Thus an 80-dB input range is compressed to 40 dB at the input to the rms-to-dc converter.

The same type of rms-to-dc converter IC is used for the

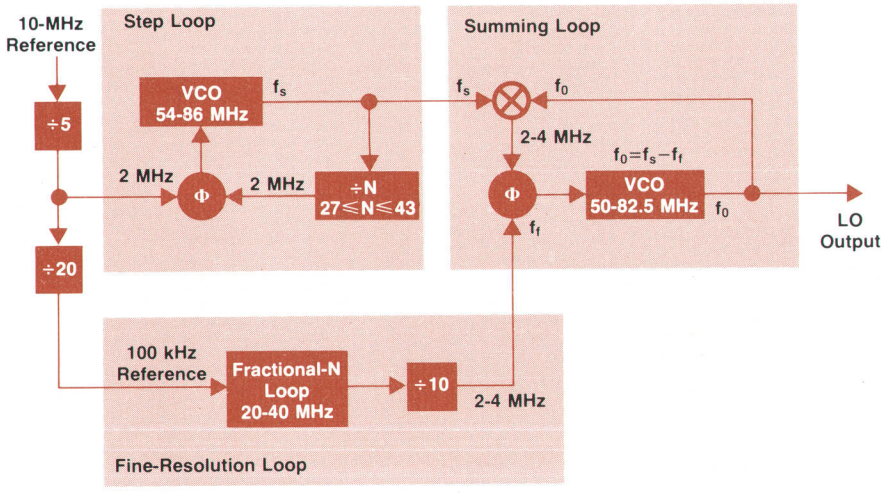

Fig. 6. *The first local oscillator synthesizer provides nine-digit frequency resolution with only three phase-locked loops. Low noise and low spurious are achieved by use of the fractional-N synthesis technique.*

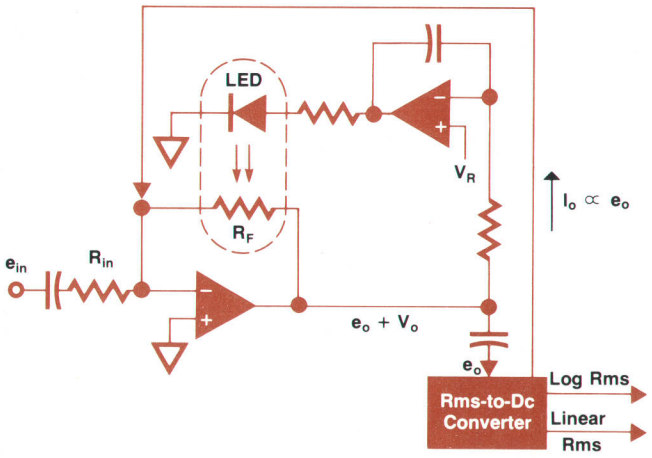

Fig. 7. *An 80-dB range of input signal levels is compressed to 40 dB by this circuit arrangement so that a commercially available rms-to-dc converter can be used as an rms detector. The converter is economical and has both log and linear outputs.*

overload detector. Here, there is no need for an 80-dB dynamic range, but there is a need to broaden the audio-frequency range of the detector to accommodate the input RF range. This is done by incoherent sampling of the input waveform at an audio rate, feeding the stretched samples to the rms-to-dc converter. The statistics of the samples are the same as the statistics of a coherently sampled waveform but there is no need for the operator to be concerned with the sampling rate (if the sampling rate were a subharmonic of the signal frequency, the samples would represent the instantaneous amplitude of the waveform at only one point on the waveform).[4] Incoherent sampling is achieved by frequency-modulating the sampling rate.

Cool Operation

Cooling an instrument to assure long-term reliability always presents a problem if the instrument is to be compact and the use of a large, noisy fan is to be avoided. Quiet, cool operation was achieved for the 3586A/B/C by using the space between the motherboard and the gasketed bottom cover as a plenum chamber pressurized by the fan. The pressurized air is allowed to flow through holes in the motherboard, up past the circuit modules, through holes in the top of the card nest, and out the sides of the instrument. The sizes of the bleed holes were chosen according to the heat dissipated by the adjacent circuits so the higher-power circuits get more air. In this way, circuits do not get air that has already been warmed by circuits elsewhere in the instrument, and the airflow for each circuit is appropriate for the amount of heat dissipated. Also, since the cards are mounted vertically in the card nest, convection aids the air flow. This arrangement provides ample cooling of the instrument with the use of a quiet, low-power fan.

Acknowledgments

As always with a complicated instrument like the 3586A/B/C, many people made contributions worthy of note. Cullen Darnell, who was engineering section manager for the earlier part of the project, provided many suggestions and insights into the FDM measurement problem. Ron Tuttle, acting as co-project leader for the last year of the project, conducted most of the environmental and specification compliance testing. The mechanical design with the innovative air distribution system was done by Mike Jewell. A special thanks goes to Mike Aken who followed the 3586A/B/C from the R&D lab to production engineering, thus insuring a smooth transition. Others on the project team include Tom Rodine, Mike Redig, Virgil Leenerts, Bob Atchley, Larry Sanders, Jerry Metz, Jerry Weibel, Steve Greer, Jon Pennington and Dave Deaver.

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Paul L. Thomas

Paul Thomas was born in Payson, Utah and attended Utah State University at Logan, graduating with a BSEE degree in 1965 and an MSEE degree in 1966. With HP's Loveland Instrument Division since 1966, he contributed to the design of the 675A/676A and 3570A Network Analyzers and served as project leader for the 3571A Tracking Spectrum Analyzer and the 3586A/B/C Selective Level Meter. There's a patent pending on the rms converter he designed for the 3586. Paul is married, has three sons (ages 11, 14, and 17), and lives in Loveland, Colorado. An active outdoorsman who enjoys hunting, fishing, and hiking, he made the two fiberglass canoes that his family uses for fishing on many summer weekends. He also serves as a consultant for radio stations in the Loveland area.

Precision Synthesizer/Level Generator Has High Spectral Purity for Telecommunications Testing

Use it alone or as a tracking signal source for the 3586A/B/C Selective Level Meter. Three versions meet CCITT, North American, and general-purpose requirements.

by Phillip D. Winslow

ON THE SURFACE, it might seem that testing a voice-grade telecommunications system would not require state-of-the-art source and analysis equipment. However, the problems incurred by stacking hundreds of amplifiers and multiplexing systems in cascade make it necessary to use precision equipment to verify component performance within the error budgets required for system operation.

Traditionally, FDM (frequency division multiplex) systems were tested by diverting traffic from part or all of the transmission channel and performing the required tests on the unloaded equipment. This approach provided a means of basic parameter testing with equipment that was scarcely more sophisticated than a wave analyzer and a tracking generator, but it suffered from the inefficiencies imposed by placing the equipment out of service.

With the development of frequency synthesized analyzers such as the HP 3745A Selective Level Measuring Set[1] and more recently the HP 3586A/B/C Selective Level Meter,[2] some of the need for off-line testing has been eliminated by measurement techniques using existing pilot signals in the FDM system.

With a new Synthesizer/Level Generator, Model 3336A/B/C (Fig. 1), extensive in-service testing can now be performed on FDM systems without causing transmission degradation in voice or data channels. The 3336A/B/C's low distortion, low spurious signal output, high amplitude accuracy, and amplitude blanking feature (the output is suppressed during frequency changes) make it fully capable of testing loaded systems.

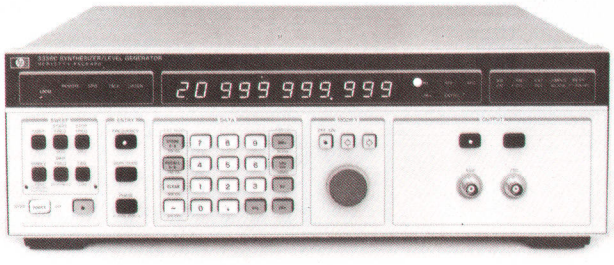


Fig. 1. *Model 3336A/B/C Synthesizer/Level Generator (3336C shown) generates precise frequencies and levels over a frequency range of 10 Hz to 20.999 999 999 MHz. Output levels are accurate within ±0.05 dB, and integrated phase noise is less than −60 dBc.*

FDM Requirements

An FDM system is a hierarchy of multiplexing stages. The European CCITT system, for example, multiplexes twelve 4-kHz voice channels to form a group. Five groups are then multiplexed to form a supergroup. At the hypergroup level, 15 supergroups are multiplexed to yield a total of 900 voice channels. Depending on the bit rate required, data transmission can be substituted for voice at the channel, group, or supergroup levels. In addition to the voice and data channels, pilot carriers are added at various points to serve as amplitude indicators and relocking signals.

The FDM hardware is set up to insert and monitor test signals at each point in the multiplexing system and at various points in the amplifiers and radio links between multiplexers. One commonly performed test is frequency response. To make this test without interrupting transmission, a tone is inserted at the input port of the device under test. The test frequency is located between voice channels to avoid interference with information being transmitted. A narrow-band analyzer is used at the output port to measure the flatness of the output as the test signal is stepped in 4-kHz increments across the band of interest.

Harmonic and spurious signals of the test generator must be down at least 50 dBc to avoid interference with information channels or pilot signals that happen to coincide with a multiple of the test generator frequency. The output of the generator must be shut off or blanked when switching frequencies to avoid sweeping through nearby channels. The amplitude transitions during blanking must be slow to avoid spectral splattering.

The accuracy of frequency response and other measurements depends on the reflection coefficient (return loss) of the source and analyzer. High return loss reduces stray reflections at test points, thereby reducing level inaccuracies and imbalances in the internal system. Gain measurements in FDM systems require a generator with good absolute accuracy in addition to flatness.

Another commonly made measurement is adjacent channel noise with loading. A carrier is injected into a voice

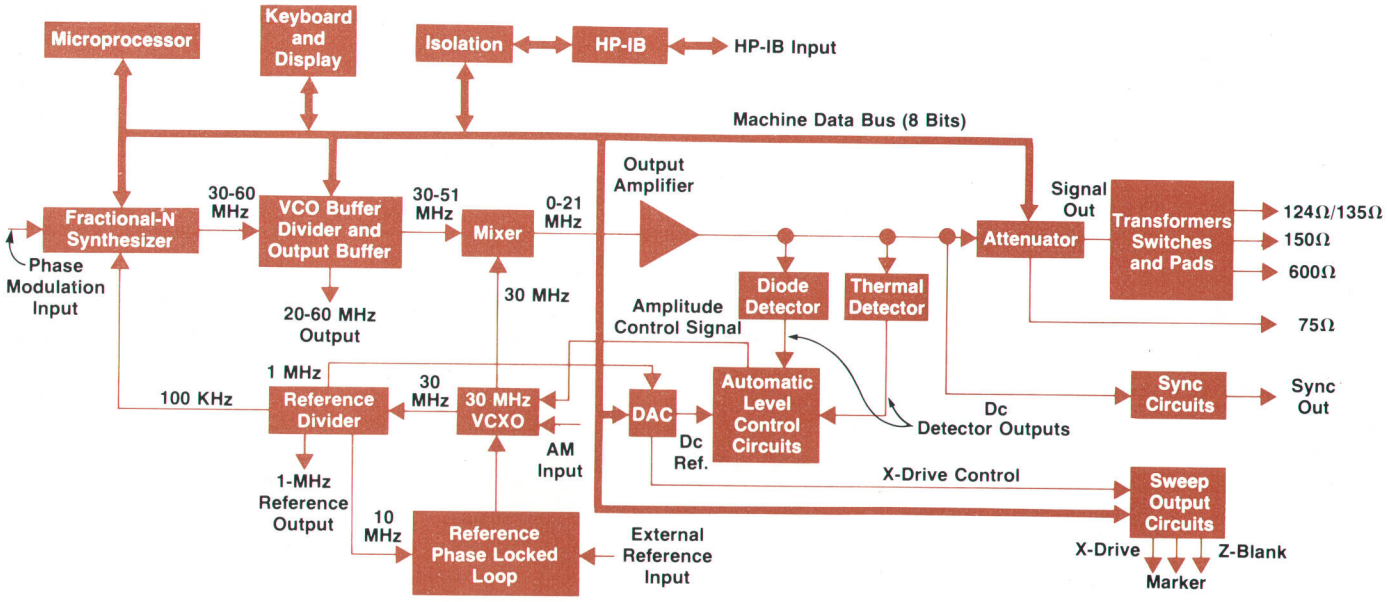


Fig. 2 *The 3336A/B/C Synthesizer/Level Generator uses the fractional-N synthesis technique to achieve low phase noise, low spurious outputs, and fast response. All operations are controlled by the microprocessor in response to commands from the front panel or the HP Interface Bus (ANSI/IEEE-488).*

On Carrier Return Loss Measurement

Return loss measurement of a conventional nonleveled source, even in the presence of the output signal, is a relatively straightforward test. A forward wave is launched by an excitation generator through a directional coupler towards the generator under test (see diagram). A spectrum analyzer at the output of the directional coupler detects the amplitude of the reflected wave. The excitation generator frequency is offset from that of the generator under test so the spectrum analyzer can distinguish the two signals.

When a generator is leveled using a servo loop, return loss takes on a slightly different meaning. The loop action offers no improvement for offset frequencies outside the leveling loop bandwidth, and only a 6-dB improvement inside the loop bandwidth. However, for passive loads, the effective output impedance depends almost entirely on the output matching resistor Z_s, but the conventional technique for measuring return loss fails to give an answer that is a function of Z_s alone.

When a small excitation signal is applied through the forward port of the directional bridge, a signal is developed at V_n given by

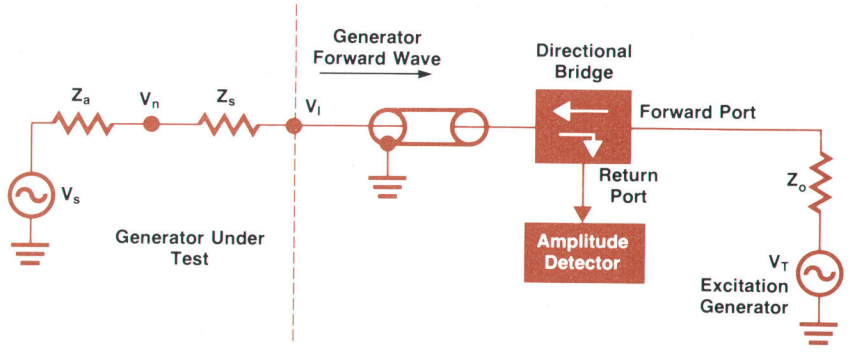
$$V_n = A\cos(\omega_1 t) + B\cos(\omega_2 t) + B\cos(\omega_3 t) + B\cos(\omega_2 t) - B\cos(\omega_3 t).$$

where A and B are related to the amplitudes of the carrier and excitation sources, V_s and V_t, ignoring servo action of the leveling loop. ω_1 is the carrier frequency, and ω_2 and ω_3 are sideband frequencies. The leveling loop then generates AM sidebands on the output carrier that cancel the AM component (second line in above equation). The resultant net forward wave out of the generator can be expressed as

$$V_l = C\cos(\omega_1 t) + D[(Z_s - Z_o)/(Z_s + Z_o)][\cos(\omega_2 t) + \cos(\omega_3 t)] + D[(Z_s - Z_o + Z_a)/(Z_s + Z_o + Z_a)][\cos(\omega_2 t) + \cos(\omega_3 t)]$$

where C and D are amplitude constants. By using a peak detector instead of a spectrum analyzer, the AM portion alone (second line) is detected from the return port of the directional bridge and is proportional to the reflection coefficient, from which the return loss can be calculated.

-Phillip D. Winslow



channel with a test generator and the noise level in the adjacent channel is measured. The 3336A/B/C's 3-kHz adjacent channel noise specification of −72 dB allows wide dynamic range measurements to be made in this test.

The inherently low phase noise of the 3336A/B/C also has an impact on data channel verification. Typically, a tone is inserted in the multiplex system and monitored at the end of the transmission channel with a phase jitter detector such as the HP 3586A/B/C. The phase jitter measurement is implemented using a phase-locked loop phase detector and a 20-to-300-Hz bandpass filter. The floor of this measurement is in part set by the source's phase noise characteristic. The 3336A/B/C's phase noise specification translates to a low 0.3° peak-to-peak phase jitter.

Internal Structure

The block diagram of the 3336A/B/C Synthesizer/Level Generator, Fig. 2, is similar to that of the 3325A Synthesizer/Function Generator.[3] The fractional-N circuits and mixer provide the same 0-to-21-MHz driving signal with low noise and low spurious signal output. The difference between the two instruments lies in the output circuits. The 3325A has a function circuit designed to produce sine, square, and triangle waveforms. A dc-coupled amplifier, optimized for minimum low-frequency distortion and settling time, provides dc offset control. The 3336A/B/C uses an automatic leveling circuit to provide flatness and amplitude accuracy. An ac-coupled amplifier is used to provide low-distortion signals over the entire 21-MHz bandwidth.

The 3336A and 3336B provide output impedances and connectors for use in the CCITT and Bell (North American) communications systems. The 3336C is designed for conventional applications requiring only 50 and 75 ohm outputs.

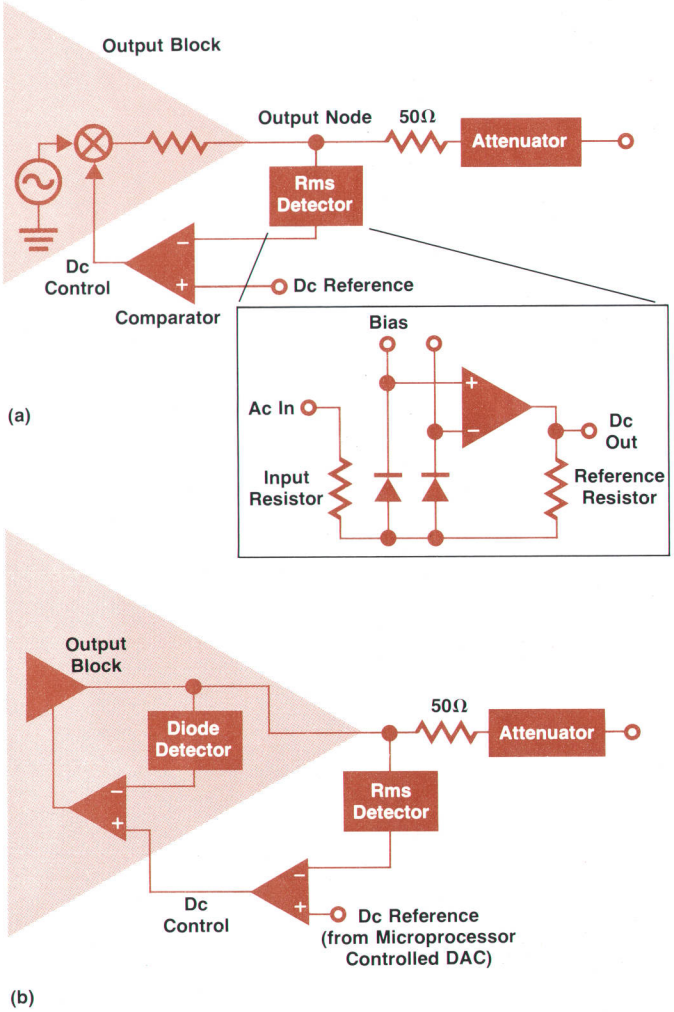


Fig. 3. *Conceptual block diagrams of the 3336A/B/C leveling loop in fast and slow leveling modes. Fast leveling, usable between 10 kHz and 21 MHz, gives ±0.15-dB flatness at sweep times as short as 0.03 second. Slow leveling can be used over the entire range of 10 Hz to 21 MHz. A front-panel button switches between the two modes.*

Leveling Loop

One approach to a level generator design is to require the mixer, associated filters, and output amplifier to have very flat frequency response, precision gain, and high return loss. This approach can present formidable design and production problems because of the accuracy and return loss required. The 3336A/B/C avoids these problems by sensing the output level near the attenuator and regulating it with control circuits. A fast leveling mode is provided for improved response time at high output frequencies. Slow leveling is used at low frequencies and when settling time is not important. Fig. 3 shows conceptual block diagrams of the servo loop in slow and fast leveling modes.

When the 3336A/B/C is in the slow leveling mode, the required accuracy and return loss are achieved with an automatic leveling control loop. The ac output of the amplifier is sensed and converted to a dc level by the rms detector and compared with a dc voltage generated by a processor-controlled digital-to-analog converter. Any error in amplitude introduced by the amplifier or offsets in the dc control circuits are detected and corrected by the comparator. The comparator is in effect an integrator and eliminates any loop error resulting from finite gain. Since the output node is servoed to a constant ac voltage and is insensitive to load, it can be considered an accurate source with zero ohms output impedance. The addition of a series 50-ohm resistor results in a flat, accurate, and high-return-loss source.

The rms converter consists of two thermally isolated heater-sensor pairs and a comparator (see page 12). The unknown ac voltage heats one pair, creating an imbalance that is sensed by the comparator. The comparator then drives the other pair into temperature balance by means of a dc voltage. Since the amounts of power dissipated in the two heater-sensor pairs are then equal, the dc voltage equals the rms value of the ac input voltage. This approach provides a means of detection that is insensitive to ambient temperature and accurate to high frequencies, but is relatively slow in response.

In fast leveling mode, another loop is placed inside the conventional loop described above. The inner loop is also a leveling loop, but uses a peak detector and different frequency shaping to decrease settling time. As a result of the increased bandwidth, this loop serves to prelevel the signal before it is seen by the outer loop. The inner loop is seen by the outer loop as a modulatable source and the slow leveling function is preserved. The difference is that sudden

A Monolithic Thermal Converter

by Peter M. O'Neill

The output leveling loop of the HP 3336A/B/C requires an accurate broadband amplitude detector to sense the actual output level. Two techniques are commonly used to measure ac voltages: peak and true-rms detection. Peak detectors have wider bandwidths but suffer from sensitivity to harmonics and absolute accuracy problems.

There are two kinds of true-rms detectors. The analog computational kind uses functional blocks to execute the square, integration, and square root functions of the defining equation. It is inexpensive, but limited to low frequencies.

Higher-frequency true-rms detectors require thermal techniques, which make use of the heating properties of ac and dc signals. Until recently, most such devices were expensive and bulky thermocouples or hybrids. Now, integrated circuit technology has made possible a low-cost, broadband, monolithic silicon, thermal rms-to-dc converter.

Operation

The thermal converter uses two heater/temperature-sensor pairs on separate thermally-isolated masses. An ac signal is applied to one heater resistor causing a rise in its temperature. A dc voltage is then fed back to a heater on an identical thermal mass until it produces a temperature equal to that of the first thermal mass as determined by a match in the temperature-sensor voltage outputs. The thermal time constants of the masses provide averaging, so that at equal voltages, the dc voltage driving one side equals the rms value of the ac voltage driving the other. The use of two sensors in a balanced configuration reduces the effects of common-mode sensor drift caused by ambient temperature and heater and sensor drift. Fig. 1 is a photograph of the converter.

Design and Fabrication

A novel feature of this thermal converter is the production of the entire thermal structure within a single crystal chip of silicon (see Fig. 2). Together the anisotropically etched mass and its support form a single-pole thermal low-pass filter that performs the mean operation in determining the root-mean-square value. The filter determines the low-frequency operating limit of the device.

The temperature sensors are high-stability junction diodes that have a voltage temperature coefficient of about −2 mV/°C when biased at constant current. Tantalum nitride thin-film resistors are used for the heaters because of their excellent temperature tracking, stability, dielectric isolation, and high-frequency response. The only significant bandwidth limitation is the inductance of the bond wires connecting the heater to the package leads.

Monolithic construction offers many advantages for this circuit. It is batch-fabricated and easily packaged. The small size and close proximity of the thermal masses results in good resistor and diode parameter matching while minimizing the effects of outside thermal gradients.

Acknowledgments

The concept and design of the device was originated by Norman Dillman of HP's Loveland Instrument Division, who also developed the silicon etching techniques and performed the system analysis.

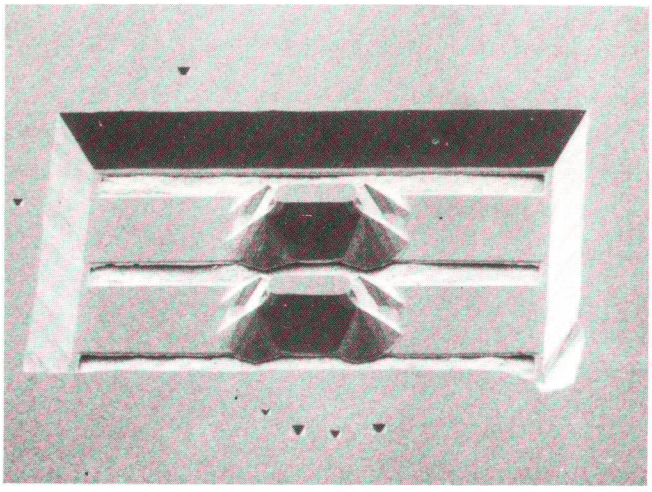


Fig. 2. *Scanning electron micrograph of the back of the thermal converter showing the anisotropically etched thermal structure.*

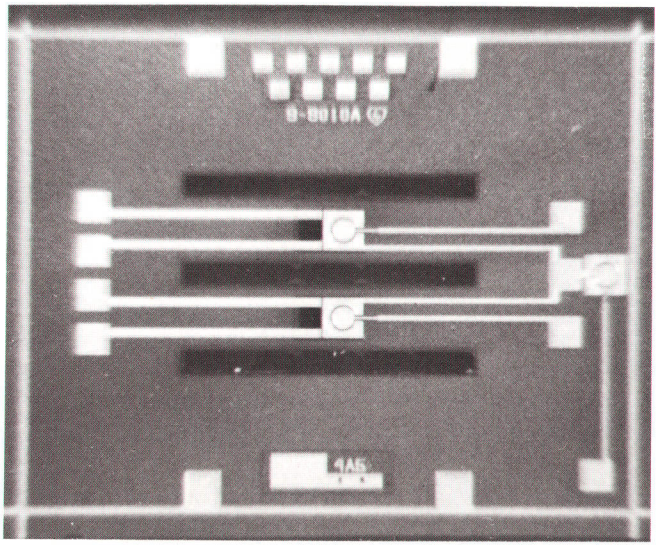


Fig. 1. *Top view of the HP thermal rms converter.*

Peter M. O'Neill

Pete O'Neill was born in Philadelphia, Pennsylvania and grew up in Wilmington, Delaware. He received his BSEE and MSEE degrees in 1977 and 1978 from Purdue University. Joining HP in 1978 as an integrated circuit process engineer, he completed development of the fabrication process for the thermal rms converter used in the 3336A/B/C, and introduced it to production. A member of IEEE, he lives in Loveland, Colorado and spends his spare time working on his new house, woodworking, skiing, bicycling, and teaching a junior high school religion class.

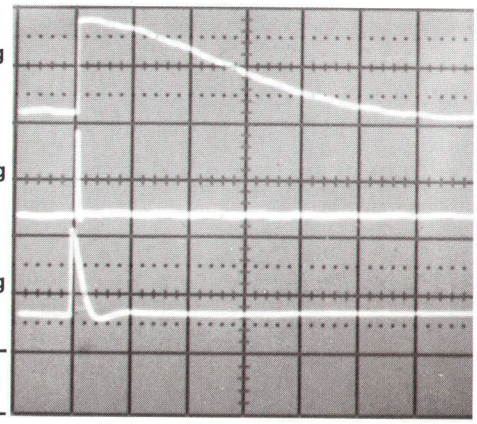


Fig. 4. *Slow and fast leveling loop responses to an output short-to-open transition.*

errors in level caused by frequency or load changes are compensated more quickly by the inner loop. The outer loop only has to correct for slow drifts in the inner loop's characteristics. Fig. 4 shows fast and slow loop responses to a short at the output of the generator. The point monitored is the output node of the amplifier.

Acknowledgments

Bill Spaulding was the original project manager. Marketing support was provided by David Ford, Bill Arrington and Paul Rumford. Norm Dillman, Bruce Huibregtse, and Pete O'Neill implemented the thermal converter. Art Dumont provided software with initial work done by Mike Price. Jim Freeman designed the mechanical portions of the instrument. Special appreciation is expressed for the guidance and support of Doug Garde.

References

1. J.R. Urquhart, "An Automatic Selective Level Measuring Set for Multichannel Communications Systems," Hewlett-Packard Journal, January 1976.
2. P.L. Thomas, this issue, page 3.
3. D.D. Danielson and S.E. Froseth, "A Synthesized Signal Source with Function Generator Capabilities," Hewlett-Packard Journal, January 1979.

Phillip D. Winslow

Phil Winslow joined HP's Loveland Instrument Division in 1974 soon after graduating from California State Polytechnic University with a BSEE degree. He's contributed to the design of the 3335A Frequency Synthesizer and served as project manager for the 3336A/B/C Synthesizer/Level Generator. Born in Yuba City, California, Phil now lives in Loveland, Colorado. He's a skier and a classical guitarist, and his interests include pipe organs, baroque music, optical communications, and high-fidelity systems.

SPECIFICATION SUMMARY

HP Model 3586A/B/C Selective Level Meter

FREQUENCY:
RANGE: 50 Hz to 32.5 MHz.
ACCURACY: $\pm 1 \times 10^{-5}$/yr ($\pm 2 \times 10^{-7}$/yr optional).
RESOLUTION: 0.1 Hz.
COUNTER ACCURACY: ±1.0 Hz + 0.1 Hz.

Signal Inputs	3586A	3586B	3586C
75Ω/10 kΩ	50 Hz to 32.5 MHz		
50Ω			50 Hz to 32.5 MHz
124Ω		10 kHz to 10 MHz	
135Ω		10 kHz to 1 MHz	
150Ω	10 kHz to 1 MHz		
600Ω/10 kΩ	50 Hz to 100 kHz		

SELECTIVITY: 3 dB Bandwidth ± 10%

3586A	3586B	3586C
20 Hz	20 Hz	20 Hz
400 Hz	400 Hz	400 Hz
1740 Hz*	2000 Hz*	3100 Hz

*3100 Hz and WTD optional

ADJACENT CHANNEL REJECTION: 75 dB.
CARRIER REJECTION: 60 dB.
PASSBAND FLATNESS: ±0.3 dB.

AMPLITUDE:
RANGE: +20 to −120 dBm.
RESOLUTION: 0.01 dBm.
LEVEL ACCURACY: For input level +20 to −80 dBm.

75/50Ω	± 0.2 dB	20 kHz to 18 MHz
124Ω	±0.35 dB	50 kHz to 5 MHz
135Ω/150Ω	±0.35 dB	50 kHz to 1 MHz
600Ω	±0.35 dB	200 Hz to 100 kHz
Wideband Power (75Ω)	± 1 dB	20 kHz to 10 MHz +20 to −45 dBm

NOISE FLOOR: (Full Scale Setting −35 to −120 dBm)

Frequency	Bandwidth	Noise Level
100 kHz to 32.5 MHz	3100, 1740, 2000 Hz	−116 dBm
	20, 400 Hz	−120 dBm
10 kHz to 100 kHz	All	−105 dBm

DYNAMIC RANGE:
IMAGE REJECTION (100-132 MHz): −80 dBc.
IF REJECTION: 15625 Hz, −80 dBc.
50 MHz, −60 dBc.
SPURIOUS SIGNALS: >1600 Hz offset, −80 dBc.
300 Hz to 1600 Hz offset, −75 dBc.
DISTORTION:
Harmonics: −70 dB below full scale, low distortion mode.
IM: −70 dB below full scale, 200 Hz to 20 kHz offset.
−75 dB below full scale, 20 kHz to 1 MHz offset.

HP-IB CONTROL: Compatible with ANSI/IEEE 488-1978.
OPTIONS:

	3586A	3586B	3586C
001 Connectors	75Ω 1.6/5.6 mm replaces BNC	75Ω WECO 124Ω WECO	--
002 Bandwidth	--	replaces mini-WECO 1740 Hz replaces 2000 Hz	--
003 Transmission Impairments	Adds: Phase jitter, 3100 Hz, WTD, Noise-with-tone, Single-Level Impulse Noise		
004 High-Stability Frequency Ref. Oscillator	$\pm 2 \times 10^{-7}$/yr Stability		

HP Model 3336A/B/C Synthesizer/Level Generator

FREQUENCY
RANGE: 10 Hz to 20.9 MHz.
ACCURACY: $\pm 5 \times 10^{-6}$ ($\pm 5 \times 10^{-8}$ optional).
RESOLUTION: 1 μHz, <100 kHz; 1 mHz, ≥100 kHz.
SIGNAL OUTPUTS:

Output	3336A	3336B	3336C
50Ω			10 Hz to 20.9 MHz
75Ω		10 Hz to 20.9 MHz	
124Ω		10 kHz to 10.9 MHz	
135Ω		10 kHz to 2.09 MHz	
150Ω	10 kHz to 2.09 MHz		
600Ω		200 Hz to 109.9 kHz	

AMPLITUDE:
RANGE:
50Ω: −71.23 to +8.76 dBm.
75Ω, 600Ω: −72.99 to +1.00 dBm.
124Ω, 135Ω: −78.23 to +1.76 dBm.
RESOLUTION: 0.01 dB.
ACCURACY: ±0.05 dB, 20°C to 30°C, at 10 kHz for 50, 75, 600Ω outputs or 50 kHz for 124, 135, 150Ω outputs (±0.08 dB 0° to 55°C).
FLATNESS: ±0.1 dB (±0.07 Option 005), at full output.
ATTENUATOR ACCURACY: ±0.1 to ±0.3 dB standard. ± 0.035 to ± 0.1 dB Option 005.
BLANKING: Soft blanking to <−85 dBm.
SPECTRAL PURITY:
HARMONIC LEVELS: −60 dB, 50 Hz to 1 MHz.
−55 dB, 1 MHz to 5 MHz.
−50 dB, 5 MHz to 20.9 MHz.
PHASE NOISE: Integrated, −64 dB, 30 kHz BW.
SSB, −72 dB, 3 kHz BW, f_c ±2 kHz.
SPURIOUS: 70 dB down or −100 dBm (−115 dBm with Option 005, depends on output and frequency).
PHASE JITTER: <±0.3° p-p.
EXTERNAL MODULATION:
AM: 50 Hz to 50 kHz, 0 to 100%.
PM: dc to 5 kHz, 0 to ±850°.
PHASE OFFSET: ±719.9° versus arbitrary starting phase or 0° relative.
FREQUENCY SWEEP:
SWEEP RANGE: Full range of signal output.
SWEEP TIME: 0.01 s to 99.9 s, depends on mode.
FLATNESS: ±0.15 dB, fast level, 0.03 s.
HP-IB CONTROL: Compatible with ANSI/IEEE 488-1978.
OPTIONS:

	3336A	3336B	3336C
001 Connectors	75Ω 1.6/5.6 mm replaces BNC	75Ω/124Ω Large WECO	
004 High-Stability Frequency Reference	$\pm 5 \times 10^{-8}$ Accuracy		
005 High-Accuracy Attenuator	Improved Attenuator Accuracy		

PRICES IN U.S.A.: 3586A (CCITT), $9200. 3586B (North American), $9200. 3586C (General-Purpose), $9100. 3336A (CCITT), $4100. 3336B (North American), $4100. 3336C (General-Purpose), $3800.
MANUFACTURING DIVISION: LOVELAND INSTRUMENT DIVISION
P.O. Box 301
815 Fourteenth Street, S.W.
Loveland, Colorado 80537 U.S.A.

Increased Versatility for a Versatile Logic State Analyzer

During analysis of program flow in a computer system, dynamically qualified multiphase clocking enables the Model 1610B to acquire for display all parts of an asynchronous transaction while excluding irrelevant events.

by Justin S. Morrill, Jr. and John D. Hansen

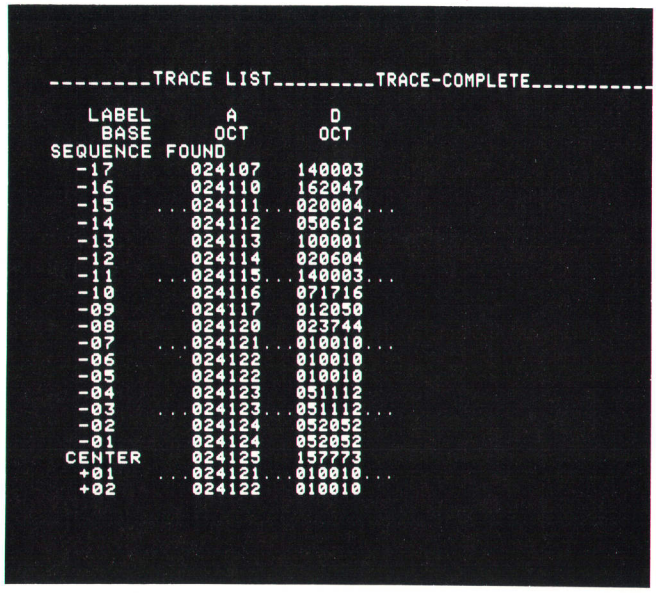
HEWLETT-PACKARD'S most powerful logic state analyzer has been the Model 1610A, first introduced in 1977.[1] With the specification of a series of program steps that must be encountered in proper order before data capture starts, this instrument can reach deep inside an executing program to capture a program sequence for analysis. The user can specify the number of times that each step must occur before the instrument starts looking for the next step so data capture can be directed to a particular branch or loop in a program.

The 1610A can be selective about the data it captures—for example, only writes to an I/O port. It can also measure time intervals between specified program steps or count the number of program steps encountered in going from one specified event to another.

New capabilities have now been added. These are found in a new version of the instrument known as the Model 1610B (Fig. 1). First among these new capabilities is multiphase clocking. This means that events that do not occur simultaneously within a digital system's instruction cycle may be captured individually and then displayed together on the same line of the program listing. For example, many buses such as I/O buses found in minicomputers use a handshake protocol when transferring information. With a single-clock analyzer, only one portion of the total transaction—the address, for example—can be traced. The 1610B with its three clock inputs can use each of the handshake signals to strobe the respective elements of the transaction into the analyzer and thereby trace the whole transaction (Fig. 2).

Another capability new to the 1610B is "sequence protect on/off." As described earlier, the user can specify several steps (up to seven) that must be encountered in a program before the instrument starts to gather data, making it possible to restrict data capture to the desired leg of a branching program. Data acquisition does not begin until the last term

Fig. 1. *Model 1610B Logic State Analyzer features multiphase clocking. Three clock inputs, each with four qualifiers, may be used to capture events in a digital system that do not occur simultaneously. A major application is decoding multiplexed buses.*



```
---------TRACE LIST---------TRACE-COMPLETE----------

   LABEL        A         D
    BASE       OCT       OCT
SEQUENCE FOUND
  -17       024107    140003
  -16       024110    162047
  -15    ...024111...020004...
  -14       024112    050612
  -13       024113    100001
  -12       024114    020604
  -11    ...024115...140003...
  -10       024116    071716
  -09       024117    012050
  -08       024120    023744
  -07    ...024121...010010...
  -06       024122    010010
  -05       024122    010010
  -04       024123    051112
  -03    ...024123...051112...
  -02       024124    052052
  -01       024124    052052
 CENTER     024125    157773
  +01    ...024121...010010...
  +02       024122    010010
```

Fig. 2. *A 1610B display of addresses and the corresponding data occurring at different times on the same processor bus.*

in the sequence is found, allowing time interval or program step counts to be made between sequence steps. This gives an overview of program operation on a macro level before specific information is obtained on a micro level in one area of code.

Once a sequence term occurs, it is stored for the rest of the measurement in a protected part of memory for later display. There are times, however, when the user would want to see the specific program steps that lead up to the final sequence term, such as the words that lead to a trap. In this case, it would be preferable to abandon protection of the sequence terms for the sake of tracing where the trap came from. The 1610B allows this tradeoff to be made.

With the sequence protect function of the Model 1610B turned off, the sequence terms are not held in a protected part of memory and data is acquired continuously as the program executes with the earliest steps spilling off the top of the 64-word memory as later steps are entered at the bottom. In the END TRACE mode, data acquisition stops when the last sequence term is found. The 63 steps leading up to the last term are then retained for display. In the CENTER TRACE mode, the instrument continues to acquire data for 32 more steps, then stops with the 31 steps preceding the last sequence term and the 32 steps following retained for display. Thus in either case, the user is able to determine the steps leading up to the last sequence term. However, earlier sequence terms are not displayed unless they happen to fall among the steps retained for display.

With sequence protect on, the 1610B functions identically to the 1610A.

Double Buffering

To understand the multiple-clocking capabilities of the 1610B, let us examine how the analyzer's front end works. A block diagram is shown in Fig. 3. Data from buses or other signal lines in the digital system under test is applied to buffer registers, four lines per register. The data is entered into four of the registers (16 lines) by one clock (J), into two of them (8 lines) by a second clock (K), and into the remaining two (8 lines) by a third clock (L). The last clock to occur is selected as the MASTER clock that transfers all the data in the 4-bit registers to the second-rank buffer storage registers. Thus, the instrument latches various portions of the input data in sequence as the clocks occur, and then the MASTER clock, the last one in the sequence, causes all the information to be transferred to the second rank where it is available for comparison to the trigger words and for transfer to the display memory.

The three clock inputs can be ORed together by the switches A and B shown in the diagram of Fig. 3. These are reed relays and thus have essentially zero propagation time and zero insertion loss. They are set open or closed at the

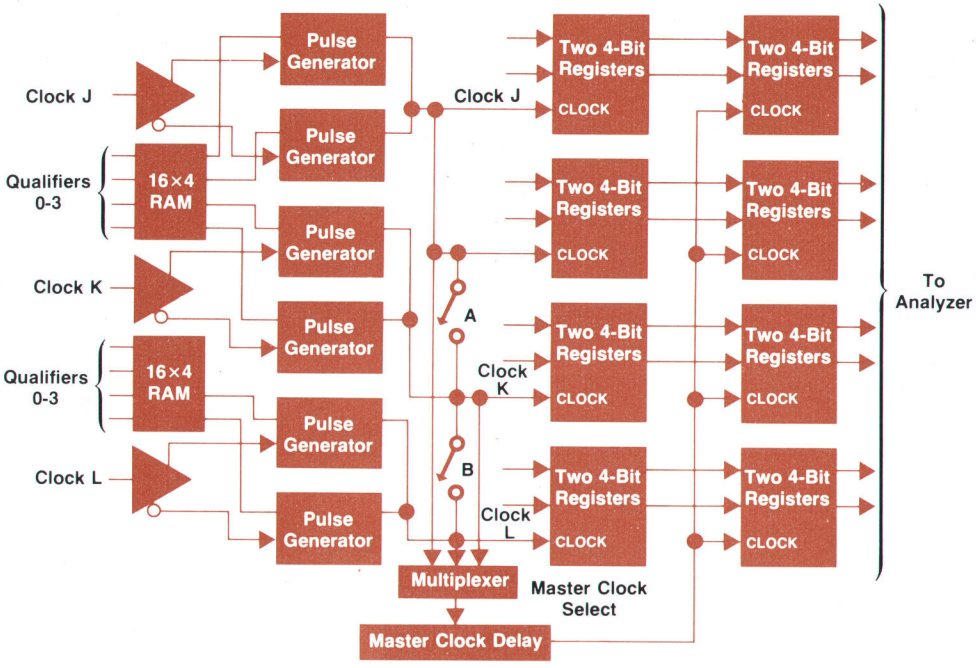


Fig. 3. *Block diagram of the 1610B front end. The last clock to occur is the MASTER clock that causes all the information in the first-rank register to be transferred to the second rank for analysis and display.*

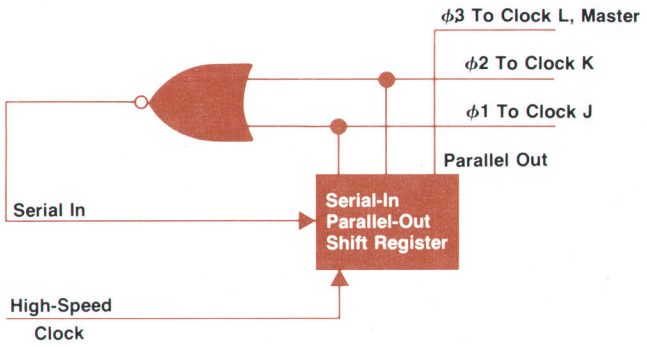


Fig. 4. *To analyze systems that operate at higher clock rates than the 1610B's maximum rate, a circuit like this can be built by the user to obtain a three-phase low-speed clock from a high-speed clock (e.g., 10 MHz 3-phase from 30 MHz). Caution: This won't work if this circuit delays the clock so much that it occurs after the data is no longer valid.*

time that the trace specifications are set up.

With switches A and B closed, the analyzer functions as a 32-bit analyzer with a single-phase clock that latches the data on all 32 input lines at the same time. With A open and B closed, the analyzer functions as a 16-16-bit analyzer with 16 bits, say the address of an instruction, latched in by the J clock and the other 16 bits, say the instruction, latched by either the K or L clocks. Though occurring at different times, both address and instruction are acquired for display.

With both A and B open, the 1610B functions in the 16-8-8 mode described earlier.

The block diagram also shows two edge-triggered pulse generators for each clock. The enable inputs on the pulse generators determine whether each clock's positive edge, negative edge, both edges, or neither functions as the latching signal. These enable conditions are determined by bits stored in a RAM. Four qualifier inputs to the analyzer make up a 4-bit address that selects one of the bit patterns stored in the RAM. Thus, through the four qualifier lines, selection of the clocking signals can be under dynamic control of the digital program being monitored. For example, one can trace program flow on several buses simultaneously and use ancillary signals that identify reads, writes, DMAs, and so forth to exclude interrupts and DMAs without using any of the 32 data input lines to make this differentiation.

Connections, 8080/1610B

Pod 4	High-Order Addresses, A15-A8
Pod 3	Low-Order Addresses, A7-A0
Pod 2 and 1	Both or Data Bus, D7-D0
	Using Part #5061-3613 Adapters
Clock Pod	Clock J and K to 02 using Part #5061-3613
	Clock L to 01
	Qual 3 DBIN Qual 2 $\overline{WR}$
	Qual 1 Sync Qual 0 No Connection

Note: Pod 1 lines for label F displayed in order are:
MEMR INP M OUT HLTA STACK $\overline{W0}$ INTA
These are the status lines of the 8080.

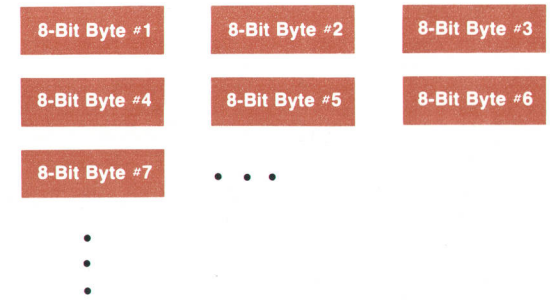


Fig. 5. *Data display using triple probing. A threefold increase in frequency can be obtained in this way, at the expense of narrowing the effective analyzer word width.*

Besides making it possible to capture and display the sequential steps of a handshake transaction simultaneously, the multiphase clocking will be especially useful for monitoring the newer microprocessors that use multiplexed buses. In several of these microprocessors, the address bus is used at different times as the data bus. Multiphase clocking enables both the address and the data involved in a transaction to be captured for display on the same program line.

Another capability provided by multiphase clocking is operation at two or three times the analyzer's normal maximum clock rate, specifically operation at 20 or 30 MHz, though with reduced word width. This is done by double or triple probing of the data lines and deriving a multiphase clock. For example, the circuit of Fig. 4 can be built by the user to obtain a 10-MHz 3-phase clock from a 30-MHz clock. The acquired data would then be displayed as shown in Fig. 5.

Stop and List

Another refinement found in the 1610B is the "stop and list" mode. In the 1610A, data in the high-speed acquisition memory is transferred to the display memory only when the trace point is found and the high-speed memory is filled. In the 1610B, if the loss of the system clock suspends operation of the system under test before the data acquisition memory is filled or a trace point is found, the user can transfer the data for display by holding down the STOP key

Format Specification Menu, 8080/1610B

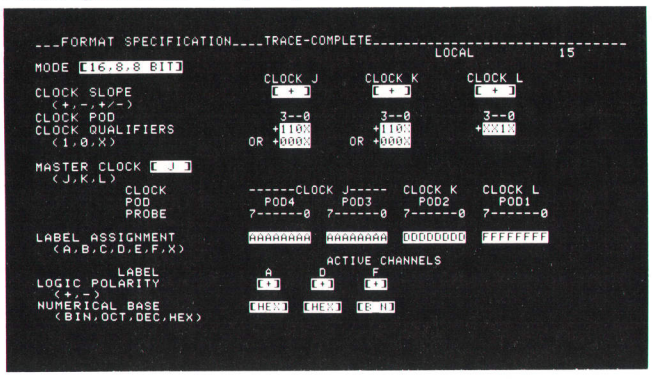


Fig. 6. *1610B setup and connections to monitor the 8080 microprocessor. Hard-to-capture 8080 status bits are easily captured and displayed with this setup.*

Connections, 8085/1610B

Pod 4	High-Order Address A8-A15						
Pod 3 and 2	Low-Order Address-Data AD0-AD7 with adapter						
Pod 1	S1	S0	IO/$\overline{M}$	$\overline{RD}$	$\overline{WR}$	STD	SID
	6	5	7	4	3	2	1

Clock Pod	Clock J	ALE	
	Clock K	$\overline{RD}$	Clock L $\overline{WR}$
	Qual 3 IO/$\overline{M}$		Qual 2 S1
	Qual 1 SO		Qual 0 No Connection

Format Specification Menu 8085/1610B

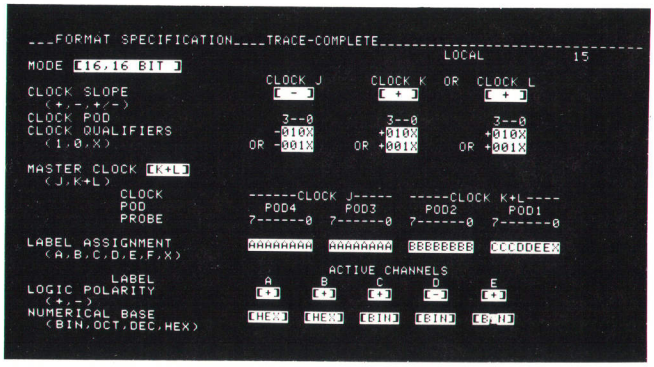


Fig. 7. *The 8085 microprocessor multiplexes part of the address with the data. The connections and setup shown allow the 1610B to monitor the 8085.*

for more than two seconds. The memory contents are then displayed with the title line reading: HISTORY AT STOP. This technique is also useful for determining what the data is doing when the analyzer fails to find the trace point.

Demultiplexing on Common Processors

Here are three examples of the use of the 1610B's multiple-phase qualified clocks for monitoring widely used processors.

8080. The 8080 is not usually thought of as a multiplexed processor, yet important information about each instruction cycle is contained in the status word that is multiplexed on the data bus at the beginning of each cycle. In many systems these status bits are difficult to get at or are only partially captured. Using a 1610B as shown in Fig. 6, the full status word can be captured and displayed. Storage qualification on this field allows the user to limit data capture to only interrupt acknowledge cycles, only stack operations, or only instruction fetches. Using the additional qualification available on the clocks, only reads or only writes on the bus can be selected.

8085. Instead of multiplexing the status bits, the 8085 multiplexes part of the address with the data. With the 1610B, the address can be entered, together with data, status, and control lines to specify the acquisition criteria. Qualification on the status lines allows selection of the machine cycles of interest, as shown in the table below. The only one not recognized is INA, which requires a clock change.

8085 Machine Cycle Chart*

Machine Cycle		Status			Control		
		IO/$\overline{M}$	S1	S0	$\overline{RD}$	$\overline{WR}$	$\overline{INTA}$
OPCODE FETCH (OF)		0	1	1	0	1	1
MEMORY READ (MR)		0	1	0	0	1	1
MEMORY WRITE (MW)		0	0	1	1	0	1
I/O READ (IOR)		1	1	0	0	1	1
I/O WRITE (IOW)		1	0	1	1	0	1
ACKNOWLEDGE OF INTR (INA)		1	1	1	1	1	0
BUS IDLE (BI)	DAD	0	1	0	1	1	1
	ACK.OF RST,TRAP	1	1	1	1	1	1
	HALT	TS	0	0	TS	TS	1

TS =High Impedance State

Fig. 7 shows how the 1610B can be set up to monitor the 8085.

LSI-11. The LSI-11** Q-Bus** is an 18-bit, asynchronous bus with data and address multiplexed. Data width is 16

*Intel Component Data Catalog, 1980.
**Registered trademark, Digital Equipment Corporation.

Connections, LSI-11 Q-Bus/1610B

Pod 4, 2	High-Order Address/Data BDAL15 - BDAL8		
Pod 3, 1	Low-Order Address/Data BDAL7 - BDAL0		
Clock Pod	Clock J	BSYNC	(Address)(−)
	Clock K	BDIN	(Read Data)(+)
	Clock L	BDOUT	(Write Data)(+)
For DMA	Clock K or L		Qual 3 BSACK
For INT Vector	Clock K or L		Qual 2 BIAK
			Qual 3 No Connection
			Qual 4 No Connection

Format Specification Menu LSI-11 Q-Bus/1610B

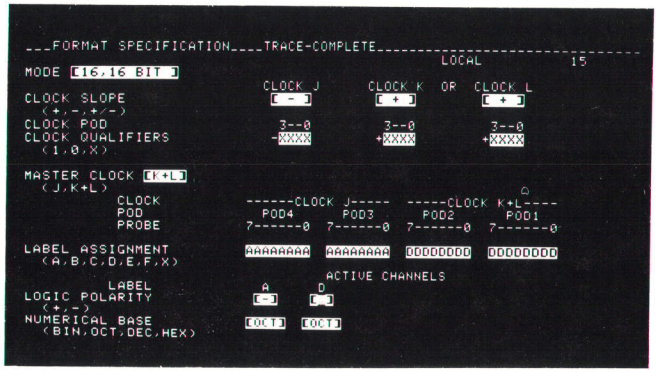


Fig. 8. *1610B setup and connections to monitor Digital Equipment Corporation's LSI-11 Q-Bus, an 18-bit asynchronous bus with addresses and data multiplexed.*

bits, with two status bits for errors. If the address is restricted to 16 bits, the 32-bit width of the 1610B can follow the machine flow. Edges of the handshake lines can be used to clock in the address and data. The upper two bits of address are lost, but if these are important, they can be exchanged with the two lower bits. For DMA operation only, or for DMA exclusion, the BSACK signal on Qualifier 3 can be used on clocks K and L. For including or excluding interrupts, the BIAK signal on Qualifier 2 can be used on clocks K and L. The interrupt-acknowledge vector is in the data field with the same address as the preceding read or write. Fig. 8 shows a 1610B setup for monitoring the LSI-11 Q-Bus.

Acknowledgments

There were many contributors to the project. The primary ones were Mike Davis as section manager, Rick Nygaard and Chris Jones for software, and Dan Kolody for marketing support. The mechanical design was done by Bobby J. Self.

John D. Hansen

John Hansen received his BSEE and MSEE degrees from Brigham Young University in 1976 and 1977. With HP since 1977, he developed the acquisition hardware and a new power supply for the 1610B Logic State Analyzer. He's a member of IEEE. Before coming to HP he served briefly as a UNESCO consultant in Rumania. A native of Richfield, Utah, John is married, has a son, and lives in Colorado Springs. He's active in his church, advises an Explorer Scout troop, owns two touring motorcycles, sings in choral groups, plays harmonica, and likes to cook.

Justin S. Morrill, Jr.

Justin Morrill has been developing logic analysis products for HP since 1972; one major patent has resulted from that work. Justin was project leader for the 1610B Logic State Analyzer and is now a group leader in the logic analysis laboratory. He's a member of ACM. Born in Lawton, Oklahoma, Justin grew up in Houston, Texas. After serving in the U.S. Army for three years, he attended Cornell and Rice Universities, receiving BS and MS degrees in electrical engineering from Rice in 1971 and 1972. He now lives in Cascade, Colorado, where he's leader of the medical rescue squad and a volunteer fireman. He's married, has two children, and enjoys backpacking and cross country skiing.

SPECIFICATIONS

HP Models 1610A/B Logic State Analyzers

Clock and Data Input

REPETITION RATE: to 10 MHz.

INPUT RC: 50 kΩ shunted by ≤14 pF at the probe tip; (10248C) 100 kΩ shunted by ≤14 pF at the probe tip.

INPUT BIAS CURRENT: ≤20 μA.

INPUT THRESHOLD: TTL, fixed at approx +1.5V; variable, ±10 Vdc.

MAXIMUM INPUT: −15 V to +15 V.

MINIMUM INPUT

SWING: 0.5 V.

CLOCK PULSE WIDTH: 20 ns at threshold level.

EDGE-TO-EDGE TIMING: (1610B) master active edge to master active edge, 100 ns; master active edge to next slave active edge, 20 ns; slave active edge to next slave or master active edge, zero.

DATA SETUP TIME: time data and clock qualifiers must be present and stable prior to active clock transition, 20 ns.

HOLD TIME: time data and clock qualifiers must be present and stable after active clock transition, zero.

Trigger and Measurement Enable Outputs

TRIGGER OUTPUT (rear panel): A 50 ns ±10 ns positive TTL level trigger pulse is generated each time the trace position is recognized. If the trace position includes a word sequence, the pulse occurs when the last word is found. Trigger outputs continue to occur each time the trigger conditions are met until a new specification is traced or the Stop key is pressed. Pulse rep-rate is 0 to 10 MHz depending on the input data rates. In continuous or compared trace modes, the internal display process blanks out pulses for 100 μs at rep rates of <20 Hz.

MEASUREMENT ENABLE OUTPUT (rear panel)

1610A, SERIAL NUMBER PREFIX 1812 OR BELOW: the positive TTL-level measurement enable output (BNC, rear panel) goes high and remains high when the analyzer is looking for a trace position and goes low when a trace position is recognized or if the Stop key is pressed. In continuous or compared trace modes the transitions repeat each time a new measurement is made.

1610A, SERIAL NUMBER PREFIX 1822 OR ABOVE AND 1610B: Two BNC rear panel outputs for TTL-level measurement enable. One BNC outputs a signal which goes high and remains high when the analyzer is looking for a trace position and goes low when a trace position is recognized or Stop key is pressed. Other BNC goes low and remains low when the analyzer is looking for a trace position and goes high when a trace position is recognized or Stop key is pressed.

General

MEMORY DEPTH: 64 data transactions, 20 transactions are displayed on screen, roll keys permit viewing all 64 transactions.

TIME INTERVAL: Resolution, 100 ns; accuracy, 0.01%; maximum time, 429.4 seconds.

EVENTS COUNT: 0 to $2^{32}-1$ events.

POWER: 100, 120, 220, 240 Vac; −10% to +5%; 48 to 61 Hz; (1610A) 260 VA max; (1610B) 280 VA max.

REAR PANEL BNC OUTPUT: 5 V, 100 mA output for logic probe or other accessories.

OPERATING ENVIRONMENT

TEMPERATURE: 0°C to 55°C.

HUMIDITY: Up to 95% relative humidity at 40°C.

ALTITUDE: To 4600 m (15 000 ft).

VIBRATION: Vibrated in three planes for 15 min. each with 0.25 mm (0.010 in) excursions for 1610A and 0.38 mm (0.015 in) excursions for 1610B, 10 to 55 Hz.

WEIGHT: (1610A) net, 26.5 kg (58.5 lb); shipping, 32.2 kg (71 lb). (1610B) net 23.8 kg (52.5 lb); shipping, 29.4 kg (65 lb).

ACCESSORIES SUPPLIED: (1610A) four 10248A data probes and one 10247A clock probe; (1610B) five 10248B/C data probes; (1610A/B) one 2.3 m (7.5 ft) power cord, one operating manual, and one service manual.

PRICES IN U.S.A.:

MODEL 1610A Logic State Analyzer, $11,000.

MODEL 1610B Logic State Analyzer, $12,500.

OPTIONS:

002: adds HP Model 9866B Thermal Printer, add $3350.

003: (1610A) adds HP-IB Interface (factory installed), add $800.

003: (1610B) adds HP-IB Interface (factory installed), add $700.

004: adds HP Model 9876A Thermal Printer, add $3950.

MANUFACTURING DIVISION: COLORADO SPRINGS DIVISION
Post Office Box 2197
1900 Garden of the Gods Road
Colorado Springs, Colorado 80901 U.S.A.

General-Purpose Module Adapts Dedicated Logic State Analyzer to Almost Any Microprocessor

Although conceived originally as a logic-state analyzer dedicated to particular microprocessors, the Model 1611A now has a general-purpose module that allows it to work with almost any microprocessor.

by Deborah J. Ogden

A NEW KIND OF LOGIC STATE ANALYZER, Model 1611A, was introduced three years ago by Hewlett-Packard.[1,2] It was the first keyboard-controlled analyzer. Keyboard control makes it possible for the user to specify much more sophisticated measurement conditions than had been possible with earlier analyzers controlled by dedicated switches and knobs. For example, instead of merely gathering sequential program steps upon occurrence of a trigger word, the 1611A can restrict data capture to very specific parts of a program sequence, such as a frequently called subroutine only when called from a specific place in the program, or just the activities at a particular I/O port.

Most important, the 1611A was optimized for measurements of microprocessor operation. Towards this end, it uses personality modules that tailor the analyzer to specific microprocessors. This simplifies the hookup of the instrument to the microprocessor since the input configuration of the probes can be prearranged; a complete hookup is accomplished simply by connecting a single DIP clip to the processor with the logic polarity, clock slope, and qualifier conditions already established for that microprocessor. Furthermore, the personality modules have the capability of converting a processor's machine language into the mnemonic assembly language of that particular processor, making it much easier to read the program sequences captured by the analyzer.

At the time that the 1611A was introduced, two personality modules were available: one for the 8080 and one for the 6800. Since then, five more have been added: the F8, Z80, 6502, 1802 and 8085 modules. However, during that time many other processors were introduced, and since it is not economically feasible to design a personality module for every microprocessor that comes along, there has been a growing demand for some means of adapting the 1611A to work with any microprocessor. This would enable those

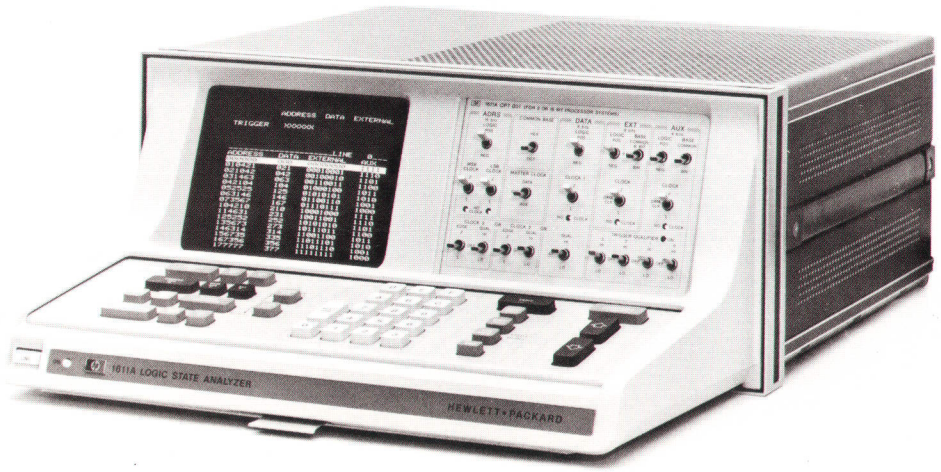


Fig. 1. *Model 1611A Logic State Analyzer with the general-purpose module (option 001) installed. A keyboard and an interactive CRT display provide a "friendly" means of setting up sophisticated measurement conditions for capture and display of state flow in microprocessor-based systems. The line shown in inverse video (black on white) on the display is the trigger word that causes the lines following to be captured for storage.*

designing with microprocessors not covered by existing modules to make use of the powerful triggering capabilities of the 1611A. Accordingly, a program was instituted to develop a general-purpose module able to handle virtually any microprocessor.

Formulating a Design

Defining such a module turned out to be a major project in itself. To begin with, it was obvious that listing program sequences in mnemonics is in direct conflict with a general-purpose thrust, since the mnemonics are processor-dependent. For the same reason, prearranged hookups could not be provided because the pin configurations of microprocessors differ.

However, other capabilities could be added to increase flexibility. One is multiple clocking, a necessity for the newer microprocessors that multiplex information on their buses. For example, one microprocessor uses an 8-bit bus for 16-bit addresses by sequencing the upper and lower bytes. On others, one bus carries both address and data information at different times. Even if a microprocessor does not multiplex its buses, some of the other pins may have different information at different times.

With the multiple clocking designed into the general-purpose module for the 1611A, one clocking event can be used to strobe in the least-significant byte of an address and another the most-significant byte (Fig. 2). A third event can be used to trigger the gathering of data in the 8-bit field known as the EXTERNAL field, and a fourth for the 4-bit AUXILIARY field. Three clocks, each of which can be qualified, can be ORed together to generate a strobe for the 8-bit DATA field. The ORed clock can be very useful because the data bus of some microprocessors is not valid on the same clocking event for every type of instruction. This clock can also be used with the other fields. For example, the EXTERNAL and AUXILIARY fields can be strobed in with the ORed clock rather than with their own dedicated strobes.

One of the clocks for the DATA, EXTERNAL, or AUXILIARY fields may be designated as the MASTER clock that strobes the gathered information into the display memory. Each line of the display may then show the activity that occurred on all the monitored lines during that instruction cycle.

Each of the seven clock inputs can be set individually to respond to either the rising or the falling edge of the corresponding clock signal.

Display Formatting

Until recently, most widely available microprocessors had an 8-bit data bus. Now, several processors with 16-bit data buses are available. This affects how the data is to be displayed on the logic analyzer. Like the dedicated modules, the general-purpose module allows collection of 36-bit words. However, since it can interrogate most any 8- or 16-bit microprocessor-based system, the option of formatting the display is provided. For 8-bit microprocessors, the usual format is a 16-bit ADDRESS field, an 8-bit DATA field, and 12 bits for other signals in the EXTERNAL and AUXILIARY fields (Fig. 3). The most desirable format for 16-bit machines is a 16-bit ADDRESS field and a 16-bit DATA field. A switch on the front panel of the general-purpose module enables the user to combine the 8-bit DATA field with the 8-bit EXTERNAL field for display as a 16-bit DATA field. Four bits are still available for auxiliary signals.

The ADDRESS and DATA fields may be displayed in either octal or hexadecimal base. The EXTERNAL and AUXILIARY fields may be displayed in binary as well as in octal or hexadecimal.

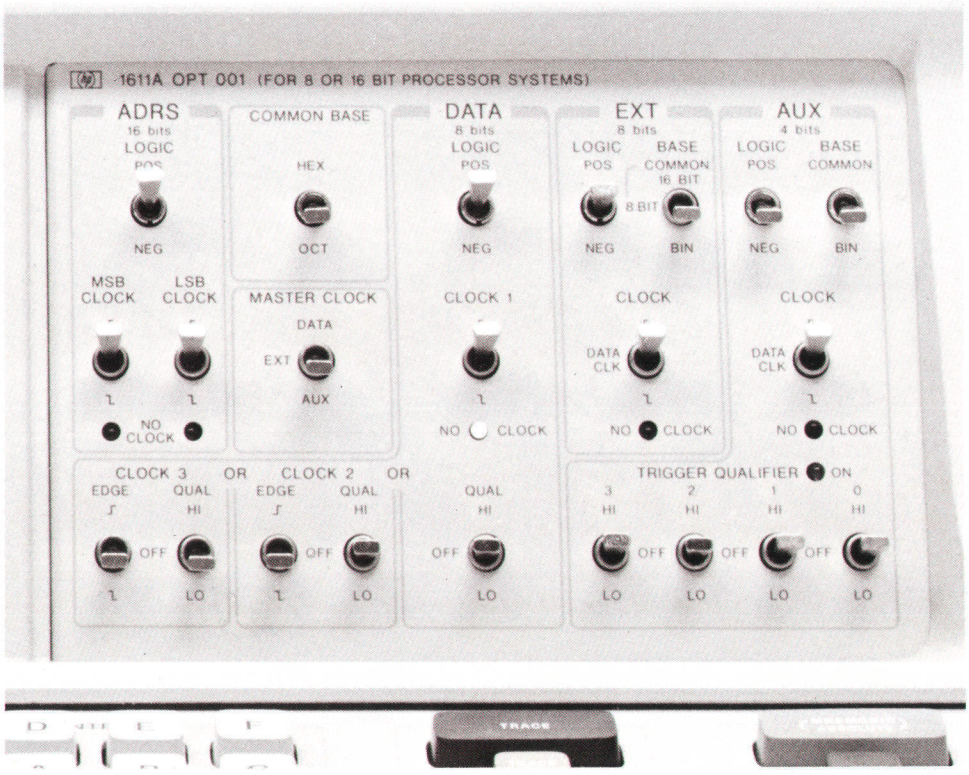


Fig. 2. *Front panel of the general-purpose module for the 1611A Logic State Analyzer. Seven clock inputs enable information on several buses to be captured for simultaneous display.*

```
          ADDRESS  DATA  EXTERNAL

TRIGGER   0F12


                          LINE  4
ADDRESS   DATA  EXTERNAL  AUX
0F16      08    FF        0011
0F17      98    FF        0011
0F18      06    FF        0001
0F1F      08    FF        0011
0F20      C8    FF        0011
0F21      50    FF        0001
0F71      00    FF        0000
0F22      08    FF        0011
0F23      40    FF        0011
0F24      68    FF        0011
0F25      78    FF        0011
0F26      70    FF        0011
0F27      90    FF        0011
0F28      EC    FF        0001
0F15      08    FF        0011
0F16      08    FF        0011
```

```
          ADDRESS  DATA  EXTERNAL

TRIGGER   0048


TRIGR OCCUR=5     PRE-TRIGR=25
                          LINE  4
ADDRESS   DATA  EXTERNAL  AUX
0040      5002            1101
0041      6000            1101
0042      6400            1101
0043      D070            1101
0070      0002            1110
0044      5C00            1101
0045      78FF            1101
0046      19FC            1101
0043      D070            1101
0070      0001            1110
0044      5C00            1101
0045      78FF            1101
0047      5100            1101
0048      7901            1101
0049      19FE            1101
0048      7901            1101
```

Fig. 3. *For an 8-bit microprocessor the display can be formatted with a 16-bit ADDRESS field, an 8-bit DATA field, and 12 bits for other signals (left). For a 16-bit microprocessor, the display can be formatted with a 16-bit ADDRESS field and a 16-bit DATA field with four bits remaining for other signals (right). The ADDRESS and DATA fields can be displayed in either octal or hexadecimal.*

Some processors operate certain buses with negative logic polarity. A switch for each of the display fields (ADDRESS, DATA, EXTERNAL and AUXILIARY) on the general-purpose module allows a choice of positive or negative logic for that field. If a switch is set for negative polarity, the software inverts data appearing on the bus before displaying it. Also, when the user enters a trigger word, it is displayed on the screen as entered, but if negative polarity has been selected for that field, the software inverts the data before loading it into the trigger comparators.

Mainframe Compatibility

The general-purpose module functions with any standard 1611A, so functions available through the 1611A keyboard are recognized. This includes trigger specifications and run commands. The only exception is that the MNEMONIC/ABSOLUTE key is disabled by the module's software.

Capabilities unique to the general-purpose module, such as clock selection, are interfaced to the user by way of the module's front panel.

Although this module will probably find most use in sorting out the complex word patterns of today's high-performance, multiplex-structured microprocessors, its capabilities also suggest its use for:

- Monitoring data flow across a parallel I/O structure;
- Investigating the status of control flags with respect to specific bus activity;
- Making time measurements across asynchronous functional circuit blocks.

Mechanical Considerations

Each type of processor has a different pin configuration. Although most come in 40-pin DIPs, there are other sizes and shapes and in the case of bit-slice processors, no single chip has a whole bus. The general-purpose module therefore has a flexible scheme for hooking up to the system under test. Altogether, the module has 46 inputs: 16 ADDRESS lines, 8 DATA lines, 8 EXTERNAL lines, 4 AUXILIARY lines, 7 clock lines, and 3 qualifiers. These are grouped into two probe pods. Connections are made with individual leads and miniature probe tips that have removable pincher-type probes (see Fig. 4). The pinchers are small enough to permit placement on adjacent pins of a standard DIP but may be removed to permit the probe tip to be slipped over the pins of a DIP-clip.

As a further convenience, the probe module to which the leads are attached can be unplugged from the probe body, exposing an edge connector that can be plugged onto a printed-circuit board that has a connector specifically wired as a test port. For particular hookups that must be "remembered," Model 10277D General Purpose Probe Interface has plug-in sockets for the two probes and a wire-wrap patch panel for prearranging the input leads.

Implementation

The block diagram of the 1611A shown in Fig. 5 indicates which functions reside on the mainframe and which are in the personality module. One of the first hardware challenges in designing the new general-purpose module was how to coordinate the gathering of data from all the various fields being strobed by clocks that may occur at different times. The problem was how to tell when every field has been gathered for one cycle, so that the information for that cycle can be stored together, and the next clocks that occur will store the fields for the next cycle. This problem was solved by allowing the user to select the MASTER clock. A switch on the front panel (Fig. 2) allows the user to indicate whether the DATA, EXTERNAL, or AUXILIARY strobe indicates "cycle complete." As shown in Fig. 6, each field is strobed into a storage buffer when its particular clock occurs, then the contents of all these buffers are latched into a second buffer when the clock chosen as MASTER occurs.

Fig. 4. *The versatile probing scheme for the 1611A Opt 001 permits a variety of methods for connecting the analyzer to the unit to be tested.*

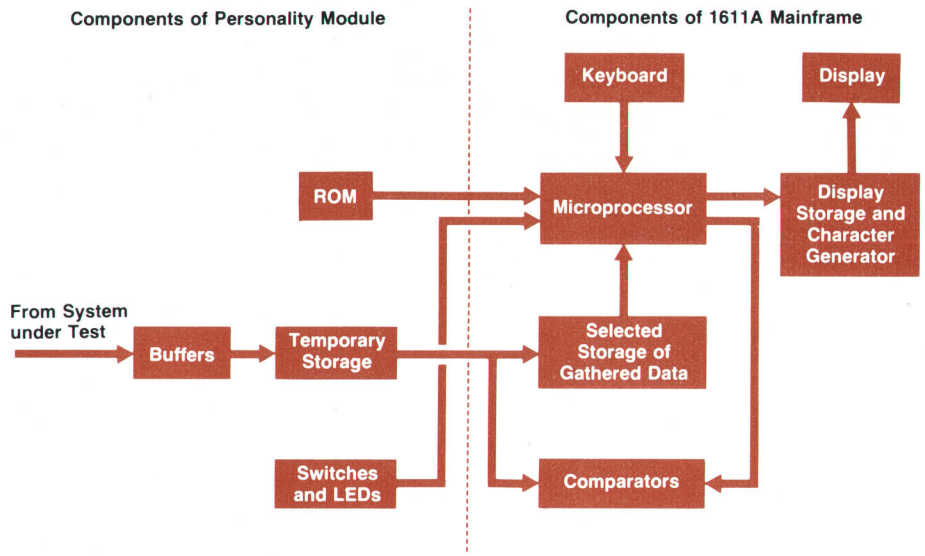


Fig. 5. *Block diagram of the 1611A Logic State Analyzer. Data enters the 1611A through a set of buffers and is temporarily stored according to the timing of the microprocessor under test. This data is then stored selectively according to user-entered conditions and is displayed by the 1611A. Keyboard-entered user conditions are formatted by the 1611A microprocessor and loaded into comparators, where they can be compared with incoming data.*

Another challenge involved the time period during which the user's data inputs must be valid with respect to the associated clocks, generally referred to as the setup and hold times (Fig. 7). The data has to be valid for some period in the vicinity of the clock, because within the logic analyzer, the data and the clocks go through buffers and other circuits that have various time delays associated with them. By the time the data is strobed into the storage buffer in the module, the various bits may not be aligned with respect to time exactly as they were when they entered the analyzer. They will, however, be lined up within certain limits. After the timing specifications of many microprocessors had been studied, it was decided to set the limits so that the hold time would be zero and the setup time as small as possible—many microprocessors do not require the data on the buses to remain valid after the corresponding clock, but most have a setup time specified.

To obtain zero hold time, the delays in the module's clock circuits must always be less than the delays in the data circuits. To assure this, Schottky TTL is used in the new module's clock paths to minimize these delays while delay lines are used in the data paths. The delay lines were chosen to assure that for worst case conditions, the data is slowed just enough to arrive at the latches simultaneously with the clocks. By computing the fastest possible clock path and the slowest possible data path, the minimum setup time was calculated to be 80 ns.

Examples

To see how the 1611A is applied to analyses of microprocessor operations with the new module (Option 001), let

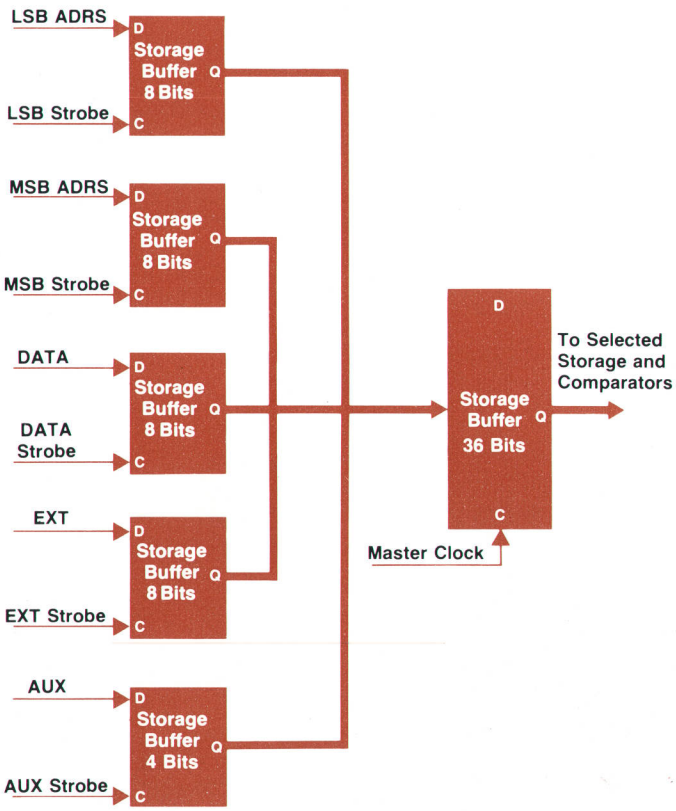
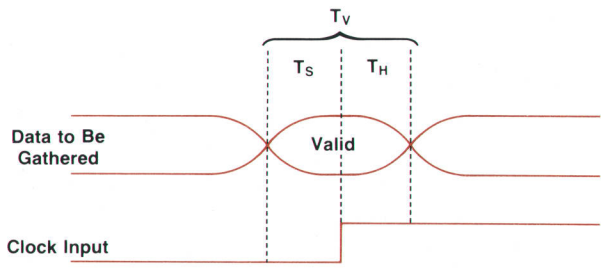


Fig. 6. *The temporary storage portion of the general-purpose module uses a double-buffering scheme to implement the master clock concept.*



T_V = Time during which data must be valid to assure it is gathered properly

T_H = Hold time

T_S = Setup time

Fig. 7. *The data to be strobed into storage must be valid at the time the strobe (clock) occurs. The timing must account for any delays encountered in the logic state analyzer's circuits.*

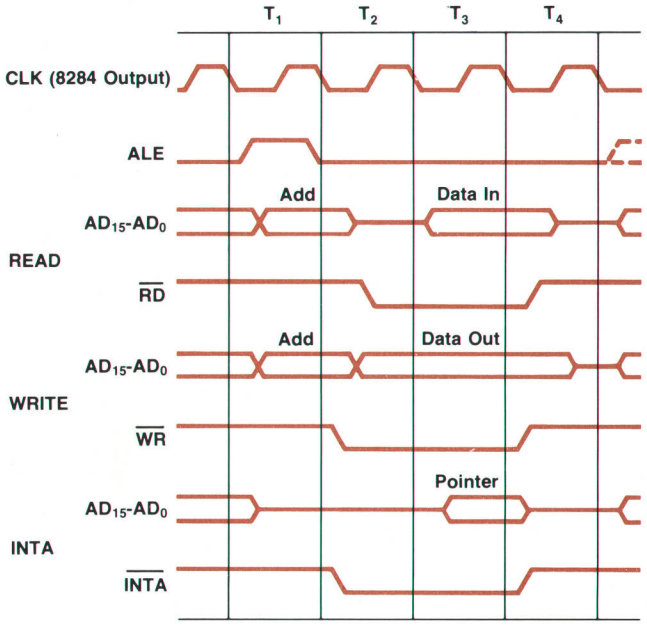


Fig. 8. *Bus timing diagram for the 8086 microprocessor.*

us look at a couple of examples. First, the Intel 8086. This is a 16-bit microprocessor that multiplexes addresses and data on one bus. Hence, the analyzer's probe lines for data are connected to the same points in the system as the probe lines for addresses. The display is formatted to contain a 16-bit ADDRESS field, a 16-bit DATA field, and four AUXILIARY bits.

Since the address information and data information are valid at different times, multiple clocks are used to gather these two fields in the same instruction cycle. As shown in the timing diagram of Fig. 8, the address field is clocked in on the falling edge of the address latch enable signal (ALE). To capture data on all memory read cycles, memory write cycles, and interrupt cycles, the data clock is the ORed combination of the rising edge of $\overline{RD}$, the rising edge of $\overline{WR}$, and the rising edge of $\overline{INTA}$.

ADDRESS DATA EXTERNAL

TRIGGER F290

ADDRESS	DATA	EXTERNAL	LINE 3 AUX
F295	95BA		1110
F296	E8FF		1110
F298	A062		1110
F29A	00EE		1110
F29C	8006		1110
0062	7D00		1110
F29E	5F00		1110
FFE8	7D00		1101
F2A0	0175		1110
005F	5F00		1110
F2A2	C95D		1110
F2A4	C208		1110
005F	5F01		1111
F2A6	0055		1110
F26C	803E		1110
F26E	5F00		1110

Fig. 9. *Trace listing of transactions in an 8086 microprocessor system presents the 16-bit ADDRESS and DATA information in hexadecimal and the AUXILIARY information in binary.*

ADDRESS DATA EXTERNAL

TRIGGER 0F12

ADDRESS	DATA	EXTERNAL	LINE 4 AUX
0F16	08	FF	0011
0F17	98	FF	0011
0F18	06	FF	0001
0F1F	08	FF	0011
0F20	C8	FF	0011
0F21	50	FF	0001
0F71	00	FF	0000
0F22	08	FF	0011
0F23	40	FF	0011
0F24	68	FF	0011
0F25	78	FF	0011
0F26	70	FF	0011
0F27	90	FF	0011
0F28	EC	FF	0001
0F15	08	FF	0011
0F16	08	FF	0011

Fig. 10. *Trace list generated while the 1611A Opt 001 monitors a SC/MP microprocessor system.*

The control lines can be monitored to provide additional insights into the processor's activity. Bit 0 of the auxiliary field can trace activity on the DT/$\overline{R}$ (data transmit/receive) line and bit 1 can be connected to the M/$\overline{IO}$ (memory/input-output) line. The two most significant bits are not used here.

The control line states for the first five lines of the listing of program flow shown in Fig. 9 indicate memory reads, and by the addresses it is seen that they are reads from ROM space. The sixth line is also a read, but it is to a RAM address. The eighth line of the listing indicates a write to an I/O port followed by signal fetches from ROM. Line 13 is a memory write to a RAM address.

To monitor an 8-bit processor such as the National SC/MP, the display is formatted to contain a 16-bit ADDRESS field, an 8-bit DATA field, an 8-bit EXTERNAL field for such data as that to and from an I/O port, and a 4-bit AUXILIARY field (Fig. 10).

The SC/MP is a 40-pin processor with 16-bit addressing

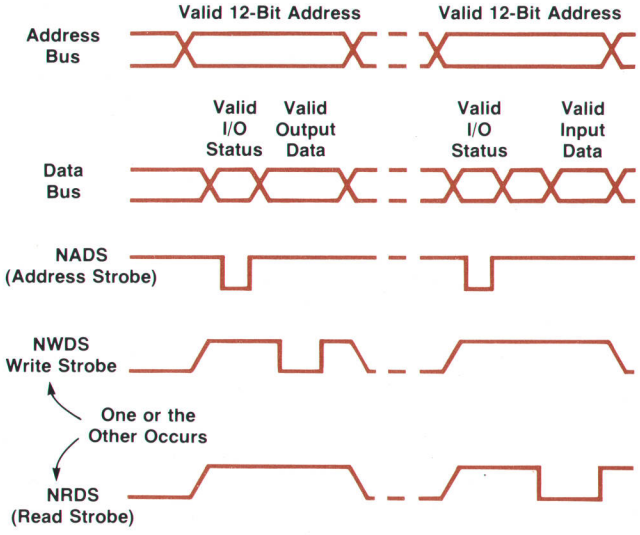


Fig. 11. *Timing diagram for the SC/MP microprocessor.*

capability, 8-bit data handling, and 22 control, clock, and flag signals. To accommodate this many signals, the chip's pinout multiplexes the data on the DATA bus with four address bits and four status bits. Therefore, when connecting the 1611A Opt 001 to the system under test, the DATA bus is double-probed. Four bits are shared by DATA and ADDRESS and the other four bits are shared by DATA and AUXILIARY.

Demultiplexing the DATA bus for the 1611A Opt 001 requires a combination of three clocks from the SC/MP. A timing diagram is shown in Fig. 11. The DATA bus, DB0-DB7, carries input data when the negative read data strobe (NRDS) is true and output data when the negative write data strobe (NWDS) is true. When the negative address ready strobe (NADS) is true, DATA bus lines DB0 through DB3 carry the upper four address bits and lines DB4 through DB7 carry processor status flags. The DATA field strobe for the 1611A is the ORed combination of the rising edge of NRDS and the rising edge of NWDS. The ADDRESS and AUXILIARY strobes are the rising edge of NADS.

Fig. 10 is a typical trace list of a SC/MP microprocessor as monitored by the 1611A Opt 001. The control lines connected to the AUXILIARY field simplify interpretation of the display. Auxiliary bit 0 monitors the RFLG line which is high (1) when data is being input to the processor. Bit 1, the instruction flag, denotes the first byte of each instruction. Monitoring these two control lines makes rapid decoding of the display possible. For example, in Fig. 10, line 1 of the display shows a 1-cycle fetch of 08 from location 0F16, lines 5 and 6 are a 2-cycle fetch of C8 and 50 followed by a 1-cycle output execution that stores 00 in location 0F71.

Acknowledgments

Jeff Smith, Justin Morrill, and Pete Rawson contributed to the module's design. Roger Molnar did the product design and Bill Furch the production engineering. Don Corson provided marketing support including invaluable assistance in the creation of this article.

Reference

1. J.H. Smith, "A Logic State Analyzer for Microprocessor Systems," Hewlett-Packard Journal, January 1977.
2. T.A. Saponas, "Firmware for a Microprocessor Analyzer," Hewlett-Packard Journal, January 1977.

SPECIFICATIONS

HP Model 1611A Option 001 Logic State Analyzer

General Purpose Personality Module

NOTE: Model 10264A personality module may be ordered separately for installation in a 1611A to provide Option 001 capability.

INPUTS

INPUT CURRENT: Approx. 200 μA logic 0 (low); approx. 20 μA logic 1 (high).
THRESHOLD: 2V min. logic 1 (high); 0.7V max. logic 0 (low); All inputs have hysteresis.
INPUT CAPACITANCE: Approx. 20 pF.

CLOCK

CLOCK RATE: dc to 2.8 MHz max. (2.2 MHz max. if installed in 1611A with serial number of 1723A or earlier). Minimum pulse width is 30 ns. No clock should occur until at least 100 ns after the master clock. The NO CLOCK indicator lights if the period between clocks exceeds 4 ms.

SETUP AND HOLD TIMES

SETUP TIME: 80 ns relative to specified clock edge.
HOLD TIME: Zero.

PRICE IN U.S.A.: 1611A Option 001, $6000. 10264A, $2000.

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Debbie Ogden holds a BS degree in computer science and an MS degree in electrical engineering, awarded by North Carolina State University in 1974 and 1976. A development engineer with HP's Colorado Springs Division since 1976, she developed the F8, Z80, and general-purpose personality modules for the 1611A Logic State Analyzer. Now with HP's Boise, Idaho Division, she's developing microprocessor software for tape drives and studying for her MBA degree part-time. Debbie is married and lives in Boise. She's a member of Toastmasters and enjoys nordic and alpine skiing, cycling, hiking, camping, and sailing her recently acquired 16-foot Hobie Cat.

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